الجامعة التكنولوجية

قسم هندسة السيطرة والنظم

مواد الامتحان التنافسي للعام الدراسي (2020−2021)

تخصص ماجستير هندسة الحاسبات

ت	اسم المـادة	تفاصيل المفردات
1	Advanced Computer Architecture (مرحلة ثالثة + رابعة)	1. Register transfer and Micro-operation, 2. Register transfer language Bus and memory transfer, 3. Arithmetic logic shift unit, 4. Arithmetic logic, and shift micro-operations, Micro-programmed control unit, Control memory, Micro-program sequencer, 5. Design of control unit. 6. Central processing unit 7. General register organization, Stack organization, Memory stack, 8. Instruction format, 9. Addressing modes, 10. Types of interrupts. 11.Memory Systems 13.Input-output organization Peripheral devices, Modes of transfer, 14.Direct memory access (DMA), Priority interrupt. 15.Parallelism in uniprocessor system 16.Comparison between parallelism and pipelining Memory systems 3. Organization, interleaving (high order, low order), Local memory types. 17. Pipelining: General principles, Arithmetic pipeline, design example pipeline adder. 18. Pipeline analysis (timing, control): Reservation table, states, Collision & collision vector analysis, hardware initiation, State diagram, Modified state diagram, Micro-programmed pipeline. 19.Vector processing: Vector instruction, vector processor, Typical Hardware architecture

-Introduction
1.   What Operating Systems Do
2.   Computer-System Organization
3.   Computer-System Architecture
4.   Operating-System Structure
5.   Operating-System Operations
6.   Computing Environments
7.   Open-Source Operating Systems Processes management
      1.   Process Concept (the process, process state ,process control block)
      2.   Operations on Processes
      3.   Process Scheduling (long term, short term scheduling, scheduling queue)
      4.   CPU scheduling
      5.   Basic concepts (CPU & I/O Burst cycle, dispatcher, preemptive & non-preemptive scheduling)
      6.   Scheduling Criteria
      7.   Scheduling Algorithms
      8.   FCFS, SJF, SRTF, RR,MLQ,MLFBQ
 	
-Process Synchronization
1.   Background
2.   The Critical-Section Problem
3.   Peterson's Solution
4.   Mutex Locks
5.   Semaphores
6.   Classic Problems of Synchronization
-Deadlocks
1.   System Model
2.   Deadlock Characterization
3.   Methods for Handling Deadlocks
4.   Deadlock Prevention
5.   Deadlock Avoidance
6.   Deadlock Detection
7.   Recovery from Deadlock
-Main Memory
	Operating System (OS)
	
	(المرحلة الرابعة)
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1. Background 2. Swapping 3. Contiguous Memory Allocation 4. Segmentation 5. Paging		
1.Network Types 2.Network Topology 3.Transmission Media 4.Network Components 5.The TCP/IP Protocol Layers: (Design Issues for the Layers) 6.The Link Layer 7.The Services Provided by the Link Layer, Error detection and Correction, Random Access Protocols 8.Transport-layer protocol 9.Transmission Control Protocol TCP (Connection Establishment), User Datagram Protocol UDP Network Layer (a) Routing Algorithms The Link-State (LS) Routing Algorithm Distance vector routing (b) IPv4 Addresses Classless Addressing Glassful Addressing (c) Computer and Network Security	Computer Networks (مرحلة رابعة)	3
1.Neural networks (NNs) : -Artificial Neuron Types of Activation functions types of NNs (Feed-forward, Feedback, Supervised and Unsupervised), and types of recall. -Learning Algorithms: Hebbians, perceptron and delta learning rules. -Generalized delta learning rule (Error back propagation algorithm for single and multiple layers. 2.Fuzzy Logic (FL) : -Introduction, Fuzzy concepts, Fuzzy sets, and Fuzzy operations. -Fuzzification, Inference Engine, Rule-Base, and	Intelligent Control Systems (مرحلة رابعة)	4

Defuzzification, -Fuzzy Logic Control (FCL). 3.Binary Genetic Algorithm (GA) . - Elements of GA, Genetic Operators, Initialization, Coding, Fitness Function ,Selection, Crossover (Mating), and Mutation		

1.Sampled Data Control Systems
  Sampling and reconstruction, properties of sampled signal, ideal Sampler, Z.O.H.
2. Analysis of Discrete Control System
   Open-loop system, closed-loop system, system time-response, steady state error analysis, mapping S-   plane /Z-plane.
3.Stability Analysis
   Bilinear transformation, Z into W, the Routh-Hurwitz criterion,   and Jury's stability test.
4. Design of Digital Controllers
   Direct design controller, dead-beat controller, PID controller,   Design and realization, response between sampling instants,   discrete Time equivalent   controller, Root locus, Modified Z- transform.
5. Time -Domain Analysis.
Impulse Response and step response for LTI processors (systems).
Digital convolution.
Difference equations.
6. Frequency-Domain Analysis (I).
Discrete Fourier Transform (DFT), DFT for periodic sequences, DFT for aperiodic digital sequence, DFT properties.
Fast Fourier Transform (FFT).
Frequency Response of LTI processor.
7. Frequency –Domain Analysis the Z-transform.
Definition and properties of the Z-transform.
Z-plane poles and Zeros.
8. Design of Recursive digital filter (IIR)
Simple design based on Z-plane poles and zeros.
Filters derived from analog designs.
	Digital Control & DSP
	(مرحلة ثالثة + رابعة)
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Frequency sampling filters.		

1. Introduction of variables, decisions, repeating a block of statements. and arrays.
2. Data structure
  Types, built in types, declaration types
3. Stack and queue
  Declaration, design functions, applications
4. Single linked list
  Declaration, design and applications
5. Graph and tree
  Declaration, design and applications
	Database and data Structure in C++
	
	(المرحلة الرابعة)
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1.Calculus limit and continuity, Differentiation, Integration, Series and sequence 2. Partial derivative. 3. Vector valued function. 4. Double integral. 5. Fourier series and Laplace transform. 6. Ordinary differential equations first order, linear set of equations.	Mathematics I مرحلة اولى + ثانية	7
1.Linear algebra and Matrices Vector, Solution of linear equations, Matrices 2.Ordinary differential equations Series solution to ODE (power series solution, Legendre polynomial, Frobenius solution and Bessel's function) and Partial differential Equations. 3.Complex Analysis 4.Numerical Analysis	Mathematics I I مرحلة ثالثة	8
Bipolar Junction Transistor (BJT) Construction, Operation, Characteristics, Configuration (C.E, C.B, C.C), Ratings. D.C. Biasing and Thermal Stability Biasing Techniques, Stability Factors, Effect of Temperature.		9

Small Signal Analysis of BJT Amplifier H-parameters Mode, re-model, Equivalent Circuit, Voltage Gain, Current Gain, Input Impedance, Output Impedance. Field Effect Transistor (FET) Construction, Types, Characteristics, Biasing and D.C. Analysis. FET Amplifiers A.C. Analysis of Common Source, Common Drain,	Electronics I مرحلة ثانية	
8086 architecture. 8086 addressing modes. 8086 instruction set. Using stack in 8086. Embedded systems definition and sample applications. Common characteristics for embedded systems. Embedded systems main parts. CISC (Complex Instruction Set Computer) versus RISC (Reduced Instruction Set Computer). Microcontroller versus microprocessor. ATmega 169 microcontroller (architecture and capabilities)	Microprocessor and embedded systems مرحلة ثالثة |+ رابعة	10