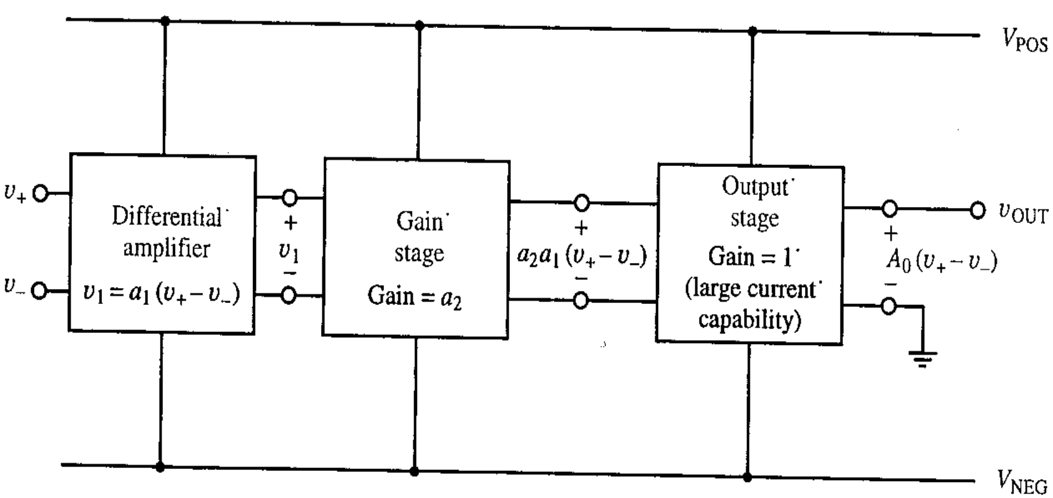
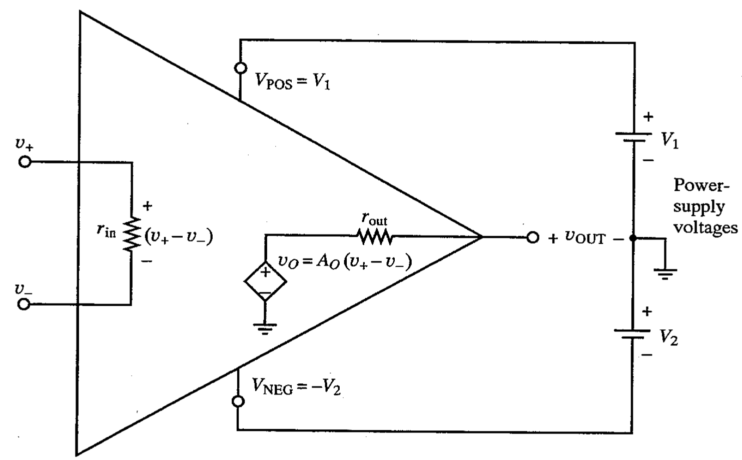
Operational Amplifiers

- An operational amplifier (called op-amp) is a specially-designed amplifier in bipolar or CMOS (or BiCMOS) with the following typical characteristics:
  - Very high gain (10,000 to 1,000,000)
  - Differential input
  - Very high (assumed infinite) input impedance
  - Single ended output
  - Very low output impedance
  - Linear behavior (within the range of $V_{NEG} < v_{out} < V_{POS}$
- Op-amps are used as generic "black box" building blocks in much analog electronic design
  - Amplification
  - Analog filtering
  - Buffering
  - Threshold detection
- Chapter 2 treats the op-amp as a black box; Chapters 8-12 cover details of op-amp design
  - Do not really need to know all the details of the op-amp circuitry in order to use it

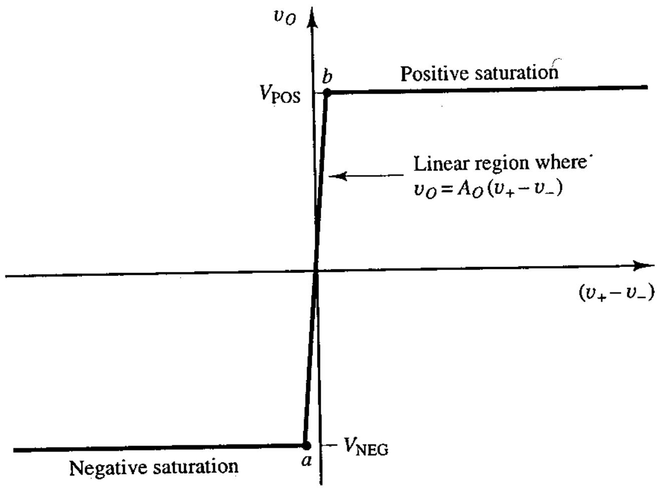
Generic View of Op-amp Internal Structure

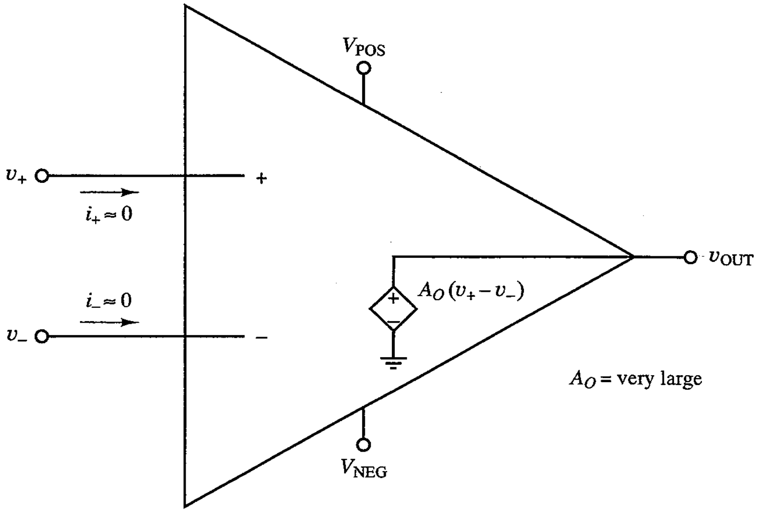
- An op-amp is usually comprised of at least three different amplifier stages (see figure)
  - Differential amplifier input stage with gain $\boldsymbol{a_1(v_+ - v_-)}$ having inverting & non-inverting inputs
  - Stage 2 is a "Gain" stage with gain $\boldsymbol{a_2}$ and differential or singled ended input and output
  - Output stage is an emitter follower (or source follower) stage with a gain = ~1 and single-ended output with a large current driving capability
- Simple Op-Amp Model (lower right figure):
  - Two supplies V_{POS} and V_{NEG} are utilized and always assumed (even if not explicitly shown)
  - An input resistance r_{in} (very high)
  - An output resistance r_{out} (very low) in series with output voltage source v_o
  - Linear Transfer function is $\mathbf{v_o = a_1 a_2(v_+ - v_-) = A_o(v_+ - v_-)}$ where A_o is open-loop gain
  - v_o is clamped at V_{POS} or V_{NEG} if $A_o (v_+ - v_-) > V_{POS}$ or $< V_{NEG}$, respectively





Ideal Op-amp Approximation

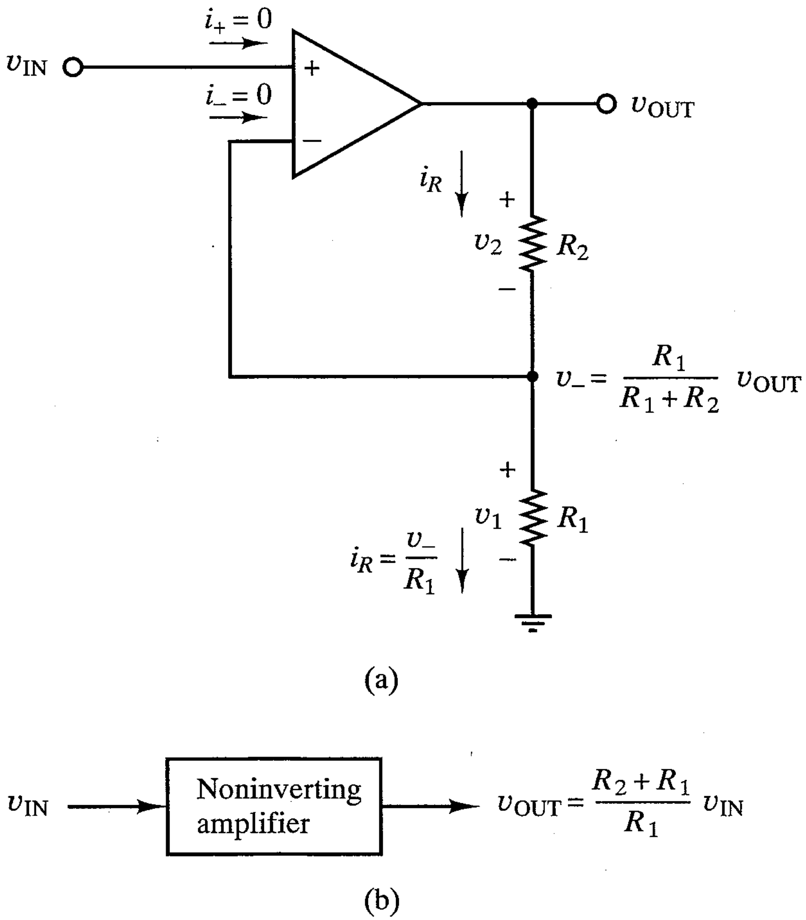




- Because of the extremely high voltage gain, high input resistance, and low output resistance of an op-amp, we use the following ideal assumptions:
  - The saturation limits of v_0 are equal V_{POS} & V_{NEG}
  - If $\mathbf{(v_+ - v_-)}$ is slightly positive, v_0 saturates at V_{POS}; if $\mathbf{(v_+ - v_-)}$ is slightly negative, v_0 saturates at V_{NEG}
  - If v_0 is not forced into saturation, then $\mathbf{(v_+ - v_-)}$ must be very near zero and the op-amp is in its linear region (which is usually the case for negative feedback use)
  - The input resistance can be considered **infinite** allowing the assumption of zero input currents
  - The output resistance can be considered to be **zero**, which allows v_{out} to equal the internal voltage v_0
- The idealized circuit model of an op-amp is shown at the left-bottom figure
- The transfer characteristic is shown at the left-top
- Op-amps are typically used in negative feedback configurations, where some portion of the output is brought back to the negative input v_-

Linear Op-amp Operation: Non-Inverting Use

Fig. 2.5 **(a) Noninverting amplifier configuration; (b) block diagram of circuit's operational function.**



- An op-amp can use ***negative feedback*** to set the closed-loop gain as a function of the circuit external elements (resistors), independent of the op-amp gain, as long as the internal op-amp gain is very high
- Shown at left is an ideal op-amp in a non-inverting configuration with negative feedback provided by voltage divider R1, R2
- Determination of closed-loop gain:
  - Since the input current is assumed zero, we can write $\mathbf{v_- = R1/(R1 + R2)v_{OUT}}$
  - But, since $v_+ =\sim v_-$ for the opamp operation in its linear region, we can write

    $v_- = v_{IN} = R1/(R1 + R2)v_{OUT}$

    or, $\mathbf{v_{OUT} = ((R1 + R2)/R1)v_{IN}}$
- We can derive the same expression by writing

  $v_{OUT} = A(v_+ - v_-) = A\{v_{IN} – [R1/(R1 + R2)]\ v_{OUT}\}$

  and solving for v_{OUT} with A>>1

  Look at Example 2.1 and plot transfer curve.

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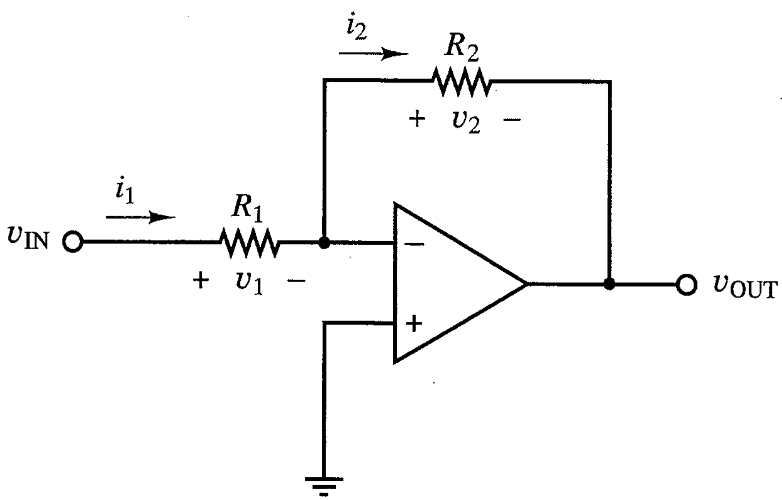
The Concept of the Virtual Short

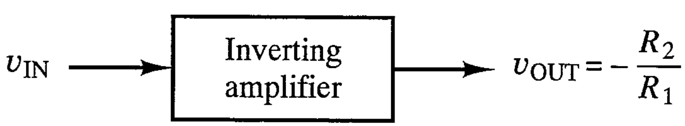
- The op-amp with negative feedback forces the two inputs v+ and v- to have the same voltage, even though no current flows into either input.
  - This is sometimes called a **"virtual short"**
  - As long as the op-amp stays in its linear region, the output will change up or down until v- is almost equal to v+
  - If v_{IN} is raised, v_{OUT} will increase just enough so that v_- (tapped from the voltage divider) increases to be equal to v_+ (= v_{IN})
    - In v_{IN} is lowered, v_{OUT} lowers just enough to make v- = v+
  - The negative feedback forces the "virtual short" condition to occur
- Look at Exercise 2.4 and 2.5
- For consideration:
  - What would the op-amp do if the feedback connection were connected to the v+ input and v_{IN} were connected to the v- input?
    - Hint: This connection is a positive feedback connection!

Linear Op-amp Operation: Inverting Configuration

Fig. 2.8 (a) Inverting amplifier configuration; (b) block diagram of circuit's operational function.



(a)



(b)

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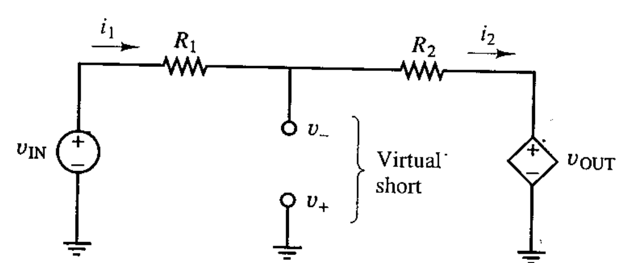
- An op-amp in the inverting configuration (with negative feedback) is shown at the left
  - Feedback is from v_{OUT} to v- through resistor R2
  - v_{IN} comes in to the v- terminal via resistor R1
  - v+ is connected to ground
- Since v- = v+ = 0 and the input current is zero, we can write
  - $i_1 = (v_{IN} – 0)/R1 = i_2 = (0 – v_{OUT})/R2$ or,

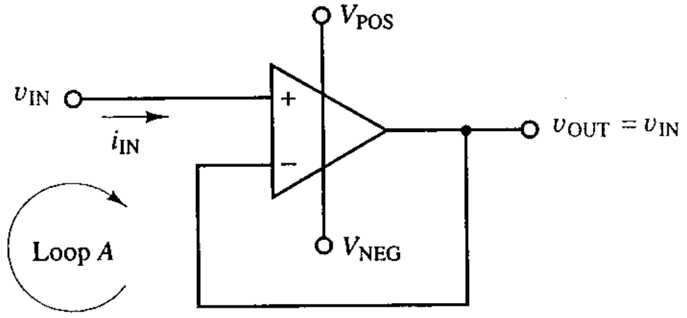
    $\mathbf{v_{OUT} = - (R2/R1)\ v_{IN}}$
- The circuit can be thought of as a resistor divider with a virtual short (as shown below)
  - If the input v_{IN} rises, the output v_{OUT} will fall just enough to hold v- at the potential of v+ (=0)
  - If the input v_{IN} drops, v_{OUT} will rise just enough to force v- to be very near 0
- Look at Example 2.2 and Exercises 2.7-2.10



Input Resistance for Inverting and Non-inverting Op-amps

- The non-inverting op-amp configuration of slide 2-4 has an apparent input resistance of infinity, since $i_{IN} = 0$ and $\mathbf{R_{IN} = v_{IN}/i_{IN} = v_{IN}/0 = infinity}$
- The inverting op-amp configuration, however, has an apparent input resistance of R1
  - since $\mathbf{R_{IN} = v_{IN}/i_{IN} = v_{IN}/[(v_{IN} – 0)/R1] = R1}$

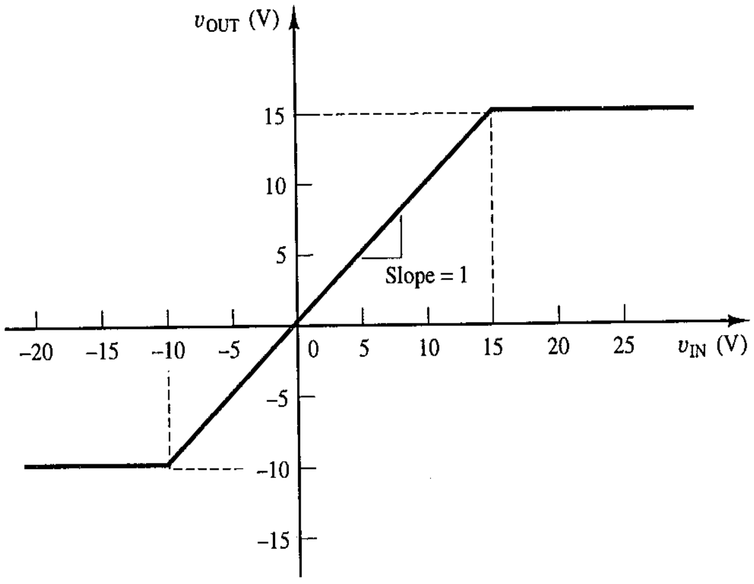
Op-amp Voltage Follower Configuration



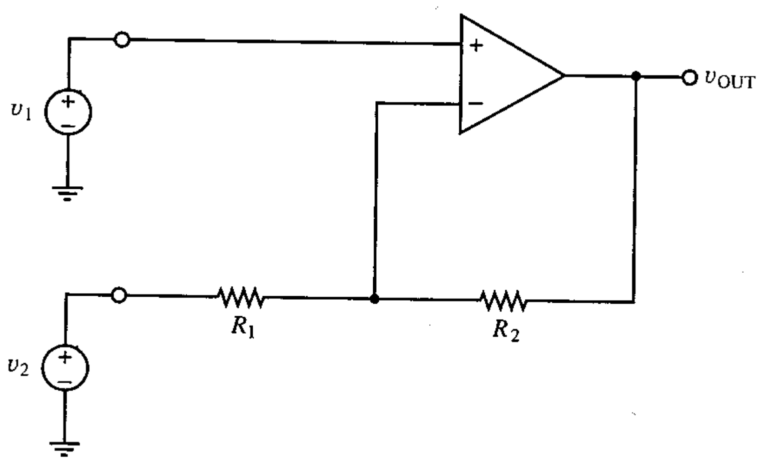
- The op-amp configuration shown at left is a voltage-follower often used as a buffer amplifier
  - Output is connected directly to negative input (negative feedback)
  - Since v+ = v- = v_{IN}, and v_{OUT} = v-, we can see by inspection that the closed-loop gain $A_o = 1$
  - We can obtain the same result by writing

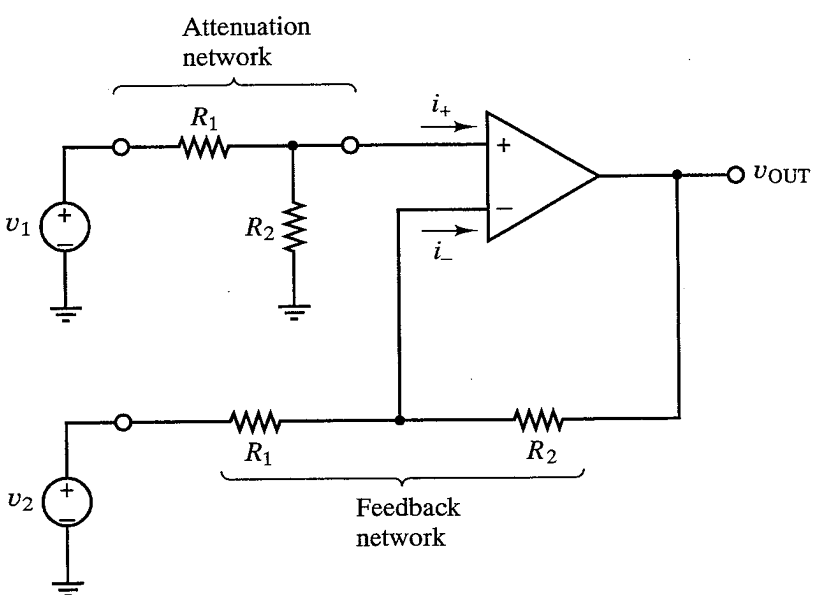
    $v_{OUT} = A\,(v_{IN} - v_{OUT})$ or

    $\mathbf{v_{OUT}/v_{IN} = A/(1 + A) = 1}$ for A >> 1
- A typical voltage-follower transfer curve is shown in the left-bottom figure for the case V_{POS} = +15V and V_{NEG} = -10V
  - For v_{IN} between –10 and +15 volts, $v_{OUT} = v_{IN}$
  - If v_{IN} exceeds +15V, the output saturates at V_{POS}
  - If v_{IN} < -10V, the output saturates at V_{NEG}
- Since the input current is zero giving zero input power, the voltage follower can provide a large power gain
- Example 2.3 in text.



Op-amp Difference Amplifier



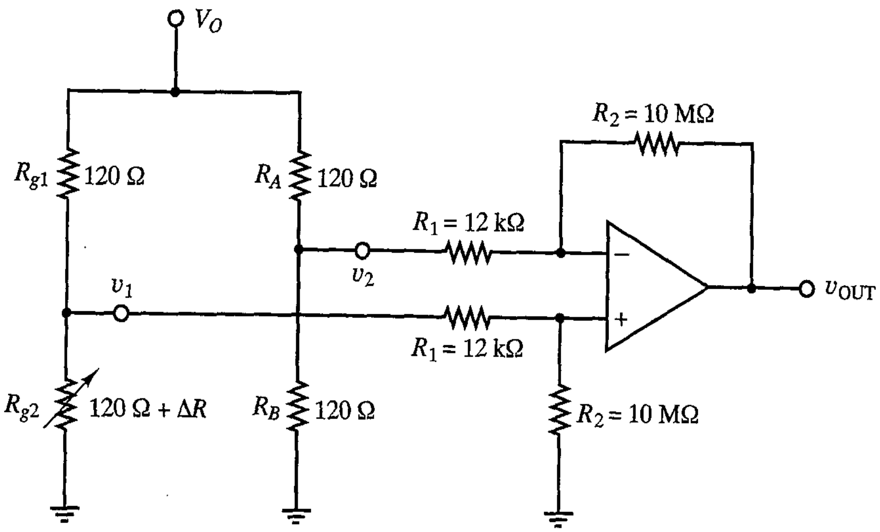


- The "difference amplifier" shown at the left-top combines both the inverting and non-inverting op-amps into one circuit
  - Using superposition of the results from the two previous cases, we can write
  - $v_{OUT} = [(R1 + R2)/R1]v_1 – (R2/R1)v_2$
  - The gain factors for both inputs are different, however
- We can obtain the same gain factors for both v_1 and v_2 by using the modified circuit below
  - Here the attenuation network at v_1 delivers a reduced input $v+ = v_1(R2/(R1 + R2))$
  - Replacing v_1 in the expression above by the attenuation factor, gives us

$$\mathbf{v_{OUT} = (R2/R1)(v_1 – v_2)}$$

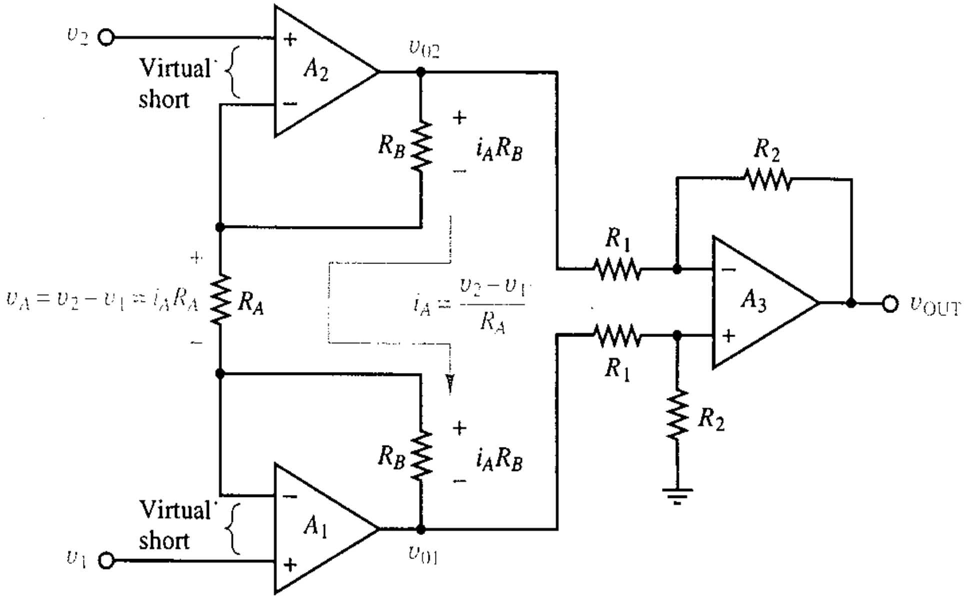
- The difference amplifier will work properly if the attenuation network resistors (call them R3 & R4) are related to the feedback resistors R1 & R2 by the relation R3/R4 = R1/R2 (i.e. same ratio)

Ex. Difference Amplifier with a Resistance Bridge



- The example of Fig's 2.14 and 2.15 in the text shows a difference amplifier used with a bridge circuit and strain gauge to measure strain.
- Operation:
  - The amplifier measures a difference in potential between v1 and v2.
  - By choosing $R_A = R_B = Rg$ (unstressed resistance of Rg1 and Rg2), it is possible to obtain an approx linear relationship between v_{OUT} and ΔL, where ΔL is proportional to the strain across the gauge.
- Design:
  - In order for the bridge to be accurate, the input resistances of the difference op-amp must be large compared to R_A, $R_{B,}$, & Rg
    - Input resistance at v1 (with v2 grounded) is R1 + R2 =~ 10 Mohm
    - Input resistance at v2 (with v1 grounded) is just R1 = 12 K due to the v1-v2 virtual short

Instrumentation Amplifier



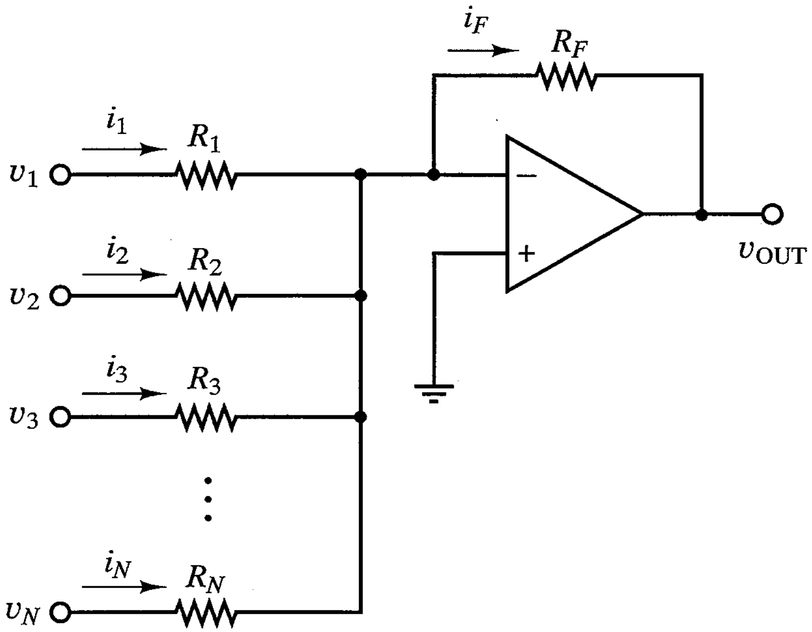
- Some applications, such as an oscilloscope input, require differential amplification with extremely high input resistance
- Such a circuit is shown at the left
  - A3 is a standard difference op-amp with differential gain R2/R1
  - A1 and A2 are additional op-amps with extremely high input resistances at v1 and v2 (input currents = 0)

- Differential gain of input section:
  - Due to the virtual shorts at the input of A1 and A2, we can write $i_A = (v2 - v1) / R_A$
  - Also, i_A flows through the two R_B resistors, allowing us to write $v_{02} - v_{01} = i_A(R_A + 2 R_B)$
  - Combining these two equations with the gain of the A3 stage, we can obtain

$$\mathbf{v_{OUT} = (R2/R1)(1 + [2R_B/R_A])(v1 - v2)}$$

- By adjusting the resistor R_A, we can adjust the gain of this instrumentation amplifier

Summation Amplifier

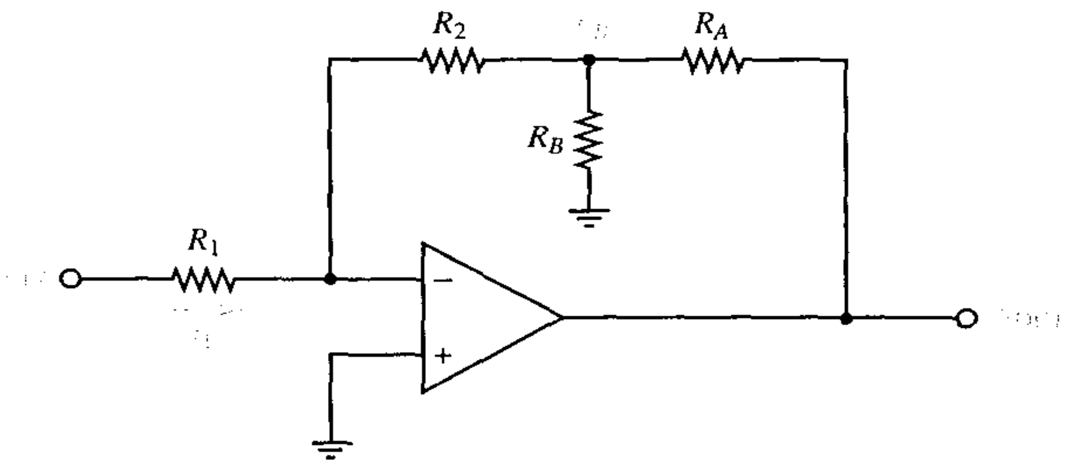


- A summation op-amp (shown at left) can be used to obtain a weighted sum of inputs v1…v_N
  - The gain for any input k is given by R_F/R_k
- If any input goes positive, v_{OUT} goes negative just enough to force the input v- to zero, due to the virtual short nature of the op-amp
  - Combining all inputs, we have

    $$\mathbf{v_{OUT} = -R_F(v_1/R_1 + v_2/R_2 + .. + v_N/R_N)}$$
  - The input resistance for any input k is given by R_k due to the virtual short between v- and v+
- Example 2.5 – use as an audio preamp with individual adjustable gain controls
  - Note effect of microphone’s internal resistance

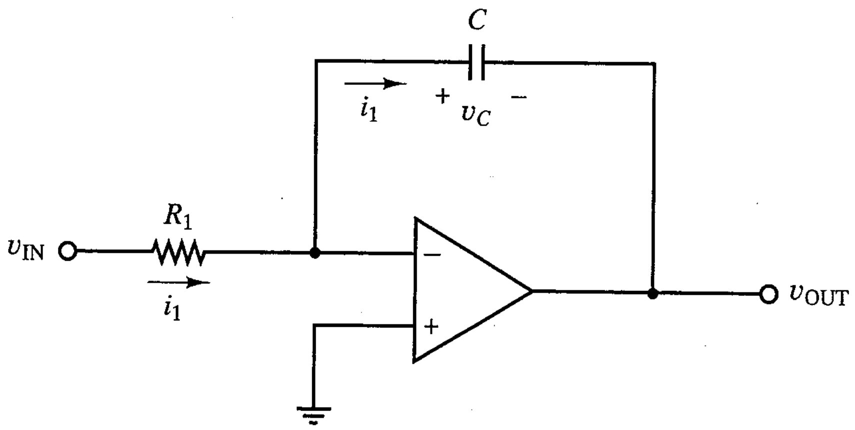
Op-amp with T-bridge Feedback Network

- To build an op-amp with high closed-loop gain may require a high value resistor R2 which may not be easily obtained in integrated circuits due to its large size
- A compromise to eliminate the high value resistor is the op-amp with T-bridge feedback network, shown below
  - R_A and R_B comprise a voltage divider generating node voltage $v_B = v_{OUT}\, R_B/(R_A + R_B)$, assuming that $R2 >> R_A||R_B$
  - Since v_B is now fed back to v-, an apparent gain $v_B/v_{IN} = -(R2/R1)$ can be written
- Combining these two equations allows us to write $v_{OUT} = -\,(R2/R1)([R_A + R_B]/R_B)v_{IN}$
- Fairly large values of closed-loop gain can be realized with this network without using extremely large IC resistors

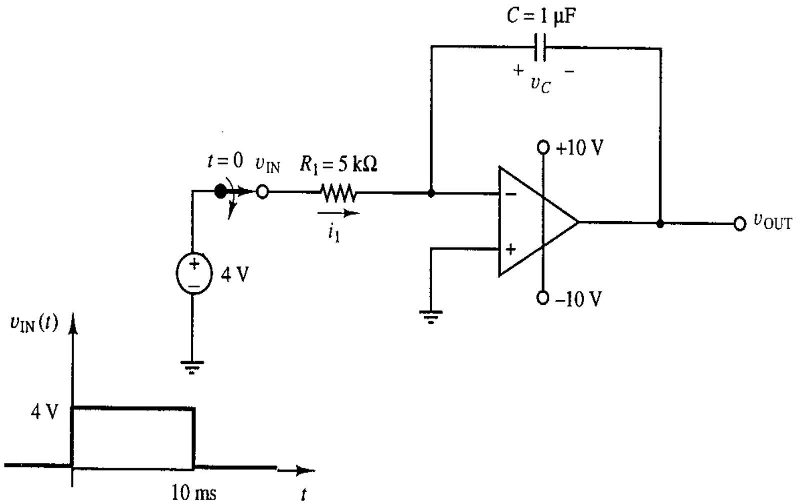


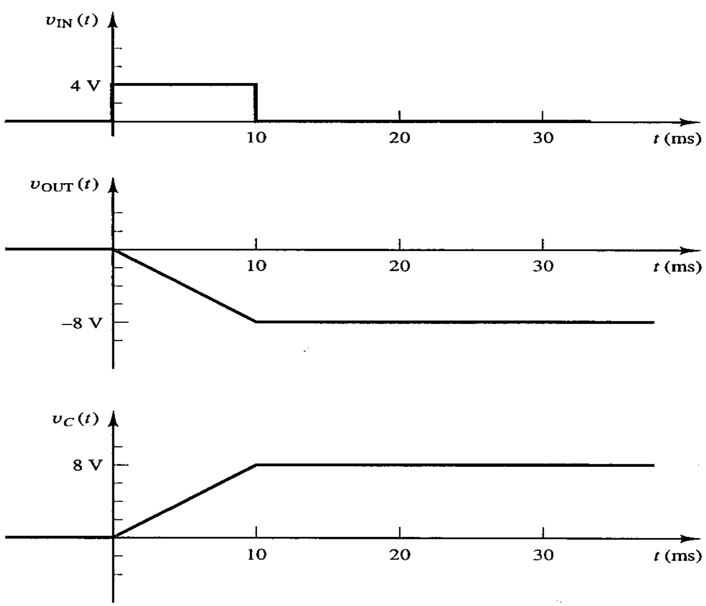
Op-amp Integrator Network

- Shown below is an op-amp integrator network
  - The output will be equal to the integral of the input, as long as the op-amp remains in its linear region
  - Due to the virtual short property of the op-amp input, we can write $i_1 = v_{IN}/R_1$
  - This current i_1 starts charging the capacitor C according to the relation $i_1 = C(dv_C/dt)$
- Since v- remains at GND, the output drops below GND as C charges and the time derivative of v_{OUT} becomes the negative of the time derivative of v_C
  - since $v_C = 0 - v_{OUT}$
- Combining the above equations, we obtain
  - $dv_{OUT}/dt = -i_1/C = -v_{IN}/R_1C$
- Solving for $v_{OUT}(t)$ and assuming C is initially uncharged, we obtain
  - $v_{OUT}(t) = (-1/R_1C) \int v_{IN}\, dt$ where the integral is from 0 to t



Op-amp Integrator Example





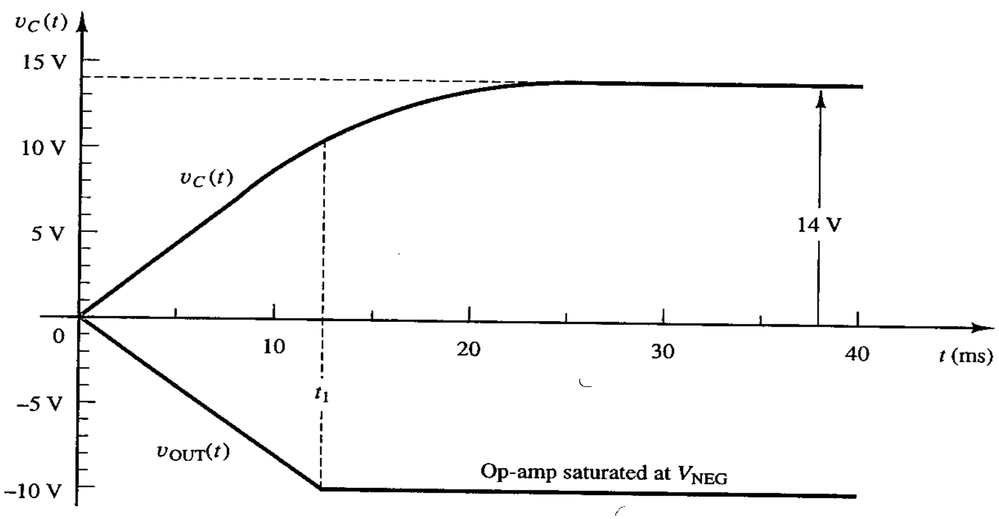
- Given an input signal of 4V square wave for 10 ms duration, what is the integrator output versus time for the integrator circuit at the left?
  - The current into the capacitor during the square wave is constant at 4V/5Kohm = 0.8 mA
  - Using the integral expression from the previous chart, the capacitor voltage will increase linearly in time $(1/R_1C)$ 4t = 0.8t V/ms during the square wave duration
  - The output will therefore reduce linearly in time by – 0.8t V/ms during the pulse duration, falling from 0 to –8 volts, as shown in the figure at left
  - Since at 10 ms the output will be –8 V > V_{NEG}, the op-amp will not saturate during the 10 ms input pulse

Op-amp Integrator Example with Long Pulse

- Consider a case with an infinitely long 4V pulse
  - The capacitor will continue to charge linearly in time, but will eventually reach 10V which will force v_{OUT} to –10V (= V_{NEG}) and saturate the op-amp (at 12.5 ms)
  - After this time, the op-amp will no longer be able to maintain v- at 0 volts
  - Since v_{OUT} is clamped at –10V, the capacitor will continue to charge exponentially with time constant R_1C until v- = +4V
    - During this time the capacitor voltage will be given by

$$\mathbf{v_C(t) = 10 + 4[1 - \exp(t_1 - t)/R_1C]} \quad \text{where } t_1 = 12.5 \text{ ms}$$

    - At $t = t_1$, v_C = 10 V and at t = infinity, v_C = 14 V
  - The resulting capacitor and output waveforms are shown below.



Op-amp as a Differentiator

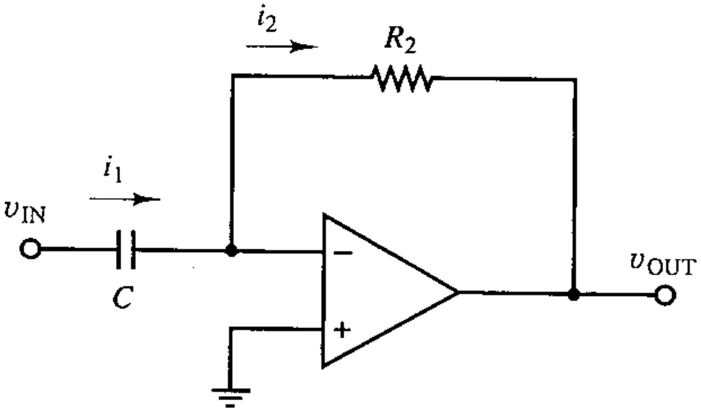
- The two op-amp configurations shown below perform the function of differentiation
  - The circuit on the left is the complement of the integrator circuit shown on slide 2-14, simply switching the capacitor and resistor
  - The circuit on the right differentiates by replacing the capacitor with an inductor
- For the circuit on the left we can write
  - $i_1 = C(dv_{IN}/dt) = i_2 = (0 - v_{OUT})/R2$ or

$$\mathbf{v_{OUT} = - R_2C\,(dv_{IN}/dt)}$$

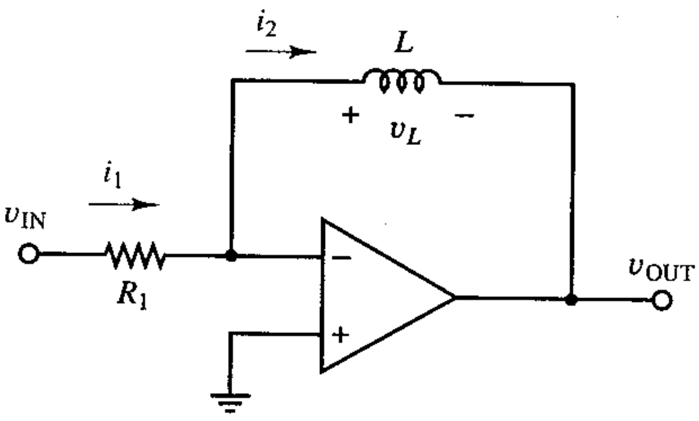
- Similarly, for the circuit on the right we can obtain

$$\mathbf{v_{OUT} = - (L/R_1)\,(dv_{IN}/dt)}$$

- By nature a differentiator is more susceptible to noise in the input than an integrator, since the slope of the input signal will vary wildly with the introduction of noise spikes.
- Do exercises 2.23 and 2.25.

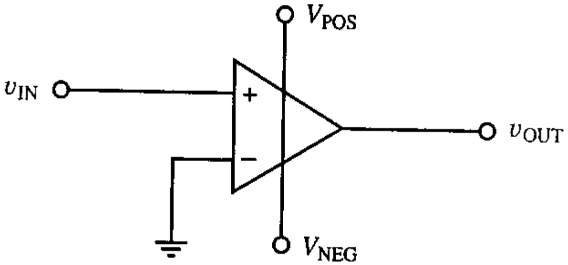


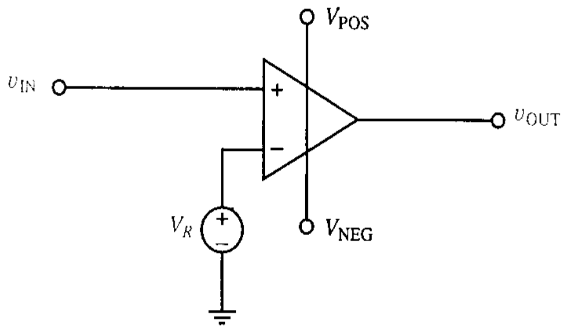
(a)



(b)

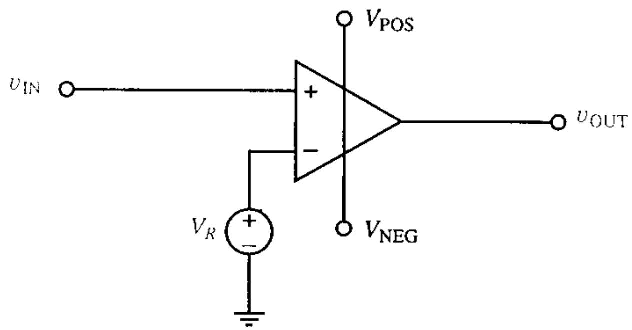
Non-Linear Op-amp Circuits

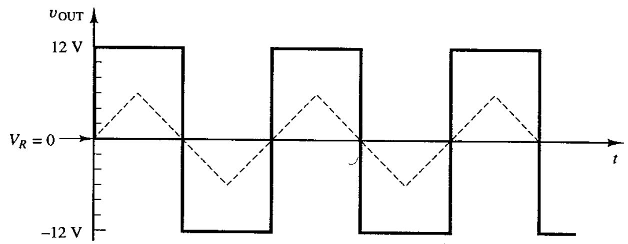




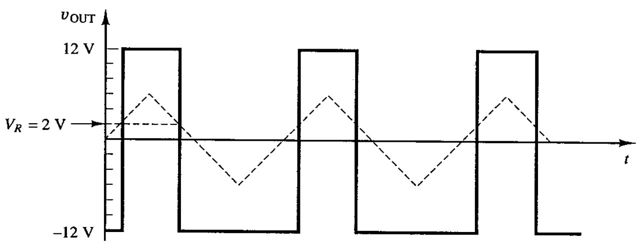
- Op-amps are sometimes used in non-linear open-loop configurations where the slightest change in v_{IN} will force the op-amp into saturation (V_{POS} or V_{NEG})
  - Such non-linear op-amp uses are often found in signal processing applications
- Two examples of such non-linear operation are shown at the left
  - Left-top is an **open-loop polarity indicator**
    - If v_{IN} is above or below GND by a few mV, v_{OUT} is forced to either positive or negative rail voltage
  - Left-bottom is an **open-loop comparator**
    - If v_{IN} is above or below V_R by a few mV, v_{OUT} is forced to the positive or negative rail voltage

Open-Loop Comparator (Example 2.8 in text)





(a)



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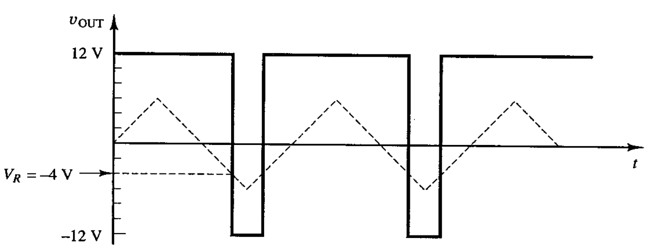
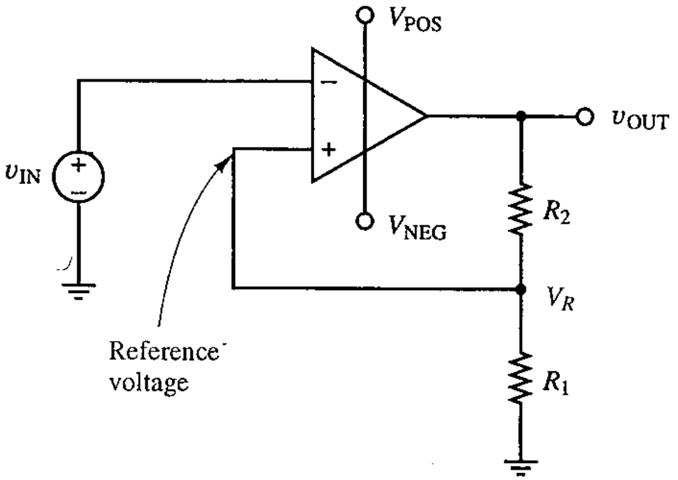
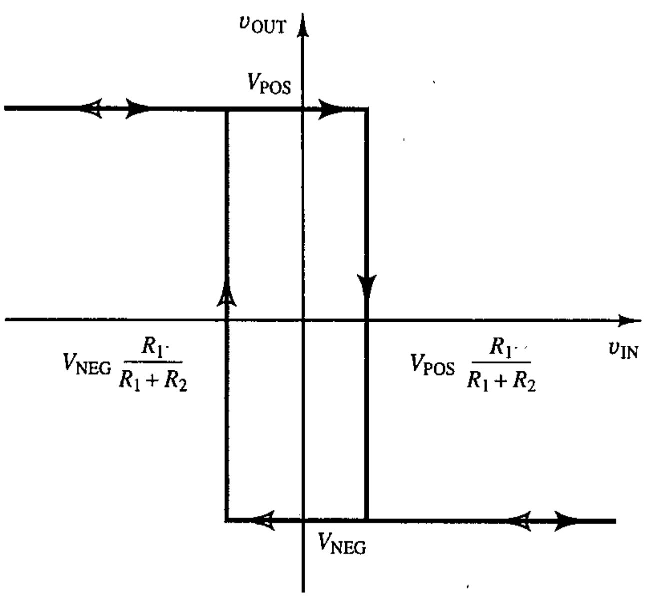


(c)

- Given the open-loop comparator shown at the left with V_{POS}= +12V and V_{NEG}= -12V, plot the output waveforms for V_R = 0, +2V, and –4V, assuming v_{IN} is a 6V peak triangle wave
- The solution is shown at the left
  - In (a) the output switches symmetrically from VPOS rail to V_{NEG} rail as the input moves above or below GND
  - In (b) the output switches between the rail voltages as the input goes above or below +2 V
  - In (c) the output switches between the rail voltages as the input varies above or below –4 V
  - The output becomes a pulse generator with adjustable pulse width
- Do Exercise 2.28.

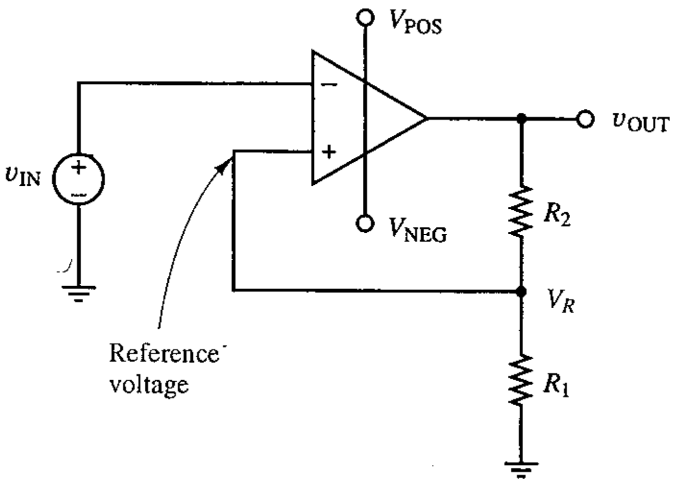
Schmitt Trigger Op-amp Circuit

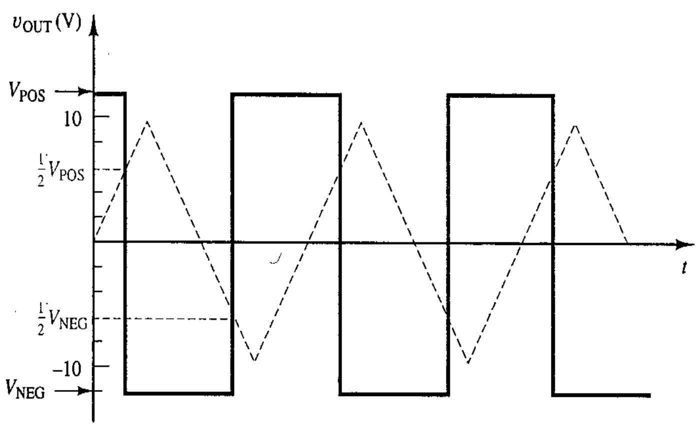




- The open-loop comparator from the previous two slides is very susceptible to noise on the input
  - Noise may cause it to jump erratically from + rail to – rail voltages
- The Schmitt Trigger circuit (at the left) solves this problem by using positive feedback
  - It is a comparator circuit in which the reference voltage is derived from a divided fraction of the output voltage, and fed back as positive feedback.
  - The output is forced to either V_{POS} or V_{NEG} when the input exceeds the magnitude of the reference voltage
  - The circuit will remember its state even if the input comes back to zero (has memory)
- The transfer characteristic of the Schmitt Trigger is shown at the left
  - Note that the circuit functions as an inverter with hysteresis
  - Switches from + to – rail when $v_{IN} > V_{POS}(R1/(R1 + R2))$
  - Switches from – to + rail when $v_{IN} < V_{NEG}(R1/(R1 + R2))$

Schmitt Trigger Op-amp Example (2.9 in text)





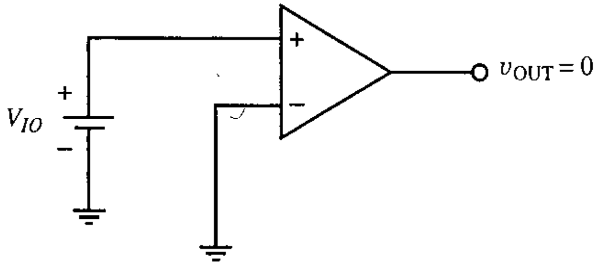
- Assume that for the Schmitt trigger circuit shown at the left, $V_{POS}/_{NEG}$ = +/- 12 volts, R1 = R2, and v_{IN} is a 10V peak triangular signal. What is the resulting output waveform?
- Answer:
  - The output will switch between +12 and –12 volts
  - The switch to V_{NEG} occurs when v_{IN} exceeds V_{POS}(R1/(R1 + R2)) = +6 volts
  - The switch to V_{POS} occurs when v_{IN} drops below V_{NEG}(R1/R1 + R2)) = -6 volts
  - See waveforms at left
- Consider the case where we start out the Schmitt Trigger circuit with v_{IN} = 0 and v_{OUT} = 0 (a quasi-stable solution point for the circuit)
  - However, any small noise spike on the input will push the output either in the + or – direction, causing v+ to also go in the same direction, which will cause the output to move further in the same direction, etc. until the output has become either V_{POS} or V_{NEG}.

Non-Ideal Properties of Op-amps:

Output Saturation and Input-Offset Voltage

Output Saturation Voltage

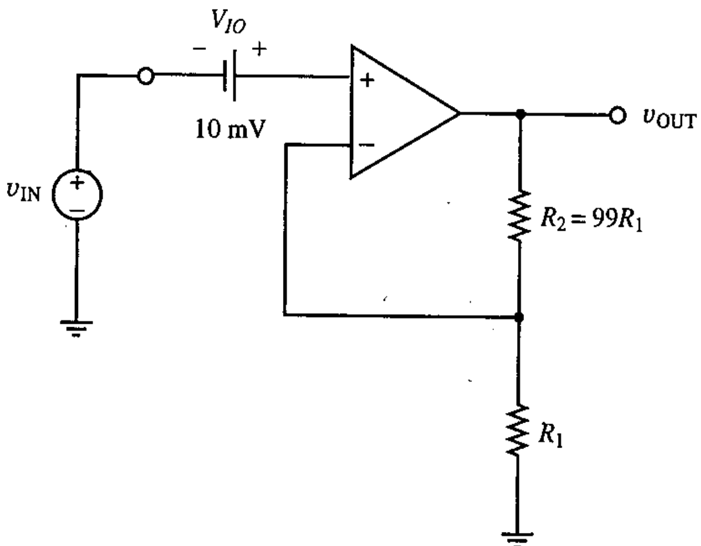
- Although we have been assuming the op-amp will saturate at the supply voltages V_{POS} and V_{NEG}, in actual practice an op-amp circuit will saturate at somewhat lower than V_{POS} and higher than V_{NEG}, due to internal voltage drops in the design
  - Emitter-follower output stage (BJT design) will drop a V_{BE}
  - CMOS design will have a similar drop



Input-Offset Voltage

- We have been assuming v+ = v- when $v_{OUT} = 0$. In actual practice, however, there is usually a small input (or output) dc offset voltage in order to force v_{OUT} to 0, under open-loop operation.
  - The input-offset voltage (labeled V_{IO} in the figure at the left) can be positive or negative and is usually small (anywhere from 1 uV to 10 mV)

Input-Offset Voltage Effect on Output Voltage



- To examine the effect input-offset voltage has on the output voltage, consider the non-inverting op-amp
  - The gain of the op-amp is (R1 + R2)/R1 = 100
  - Assume the input voltage is modeled adequately by a source V_{IO} = +/- 10 mV
  - Then, we can write that the output voltage is given by

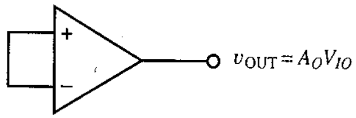
    $\mathbf{v_{OUT} = (v_{IN} + V_{IO})(R1 + R2)/R1}$

    $\mathbf{= 100\ v_{IN} +/- 1\ volt}$
  - Thus, a 10 mV input-offset causes a 1V offset in v_{OUT}
- *Exercise 2.32*: Show that the above equation applies even if V_{IO} is placed in series with the v- input, instead of the v+ input.
  - Using the virtual short condition, we can write

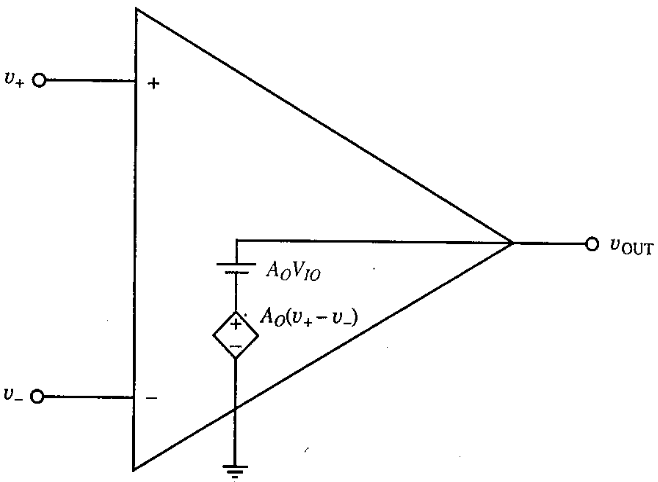
    $v_{OUT}[R1/(R1 + R2)] + V_{IO} = v_{IN}$ or

    $v_{OUT} = (R1 + R2)/R1)(v_{IN} + V_{IO})$ → same as above!
- *Exercise 2.33*: What is the output of an inverting op-amp if the effect of input offset is considered?
  - Based on the inverting op-amp circuit of slide 2-6, we can write $i_1 = (v_{IN} – V_{IO})/R1 = i_2 = (V_{IO} – v_{OUT})/R2$
  - or, $\mathbf{v_{OUT} = - (R2/R1)\ v_{IN} + V_{IO}\ (R1 + R2)/R1}$

Output-Offset Voltage and Nulling Out Offset



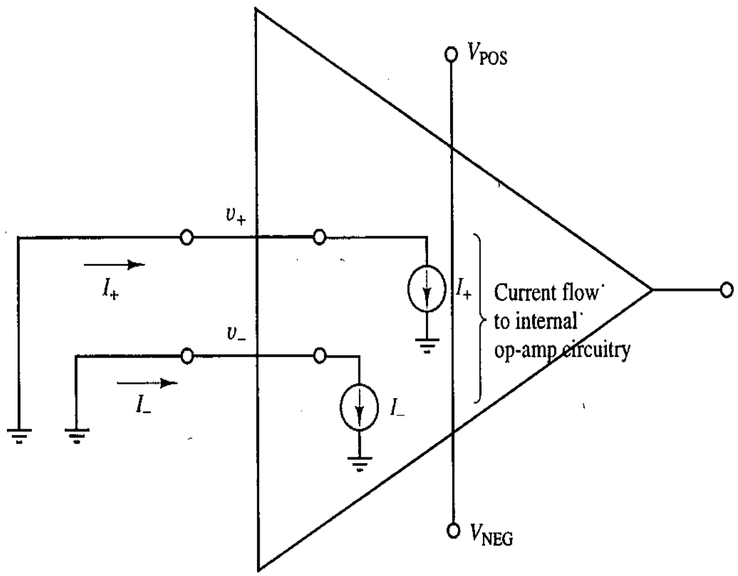
(a)

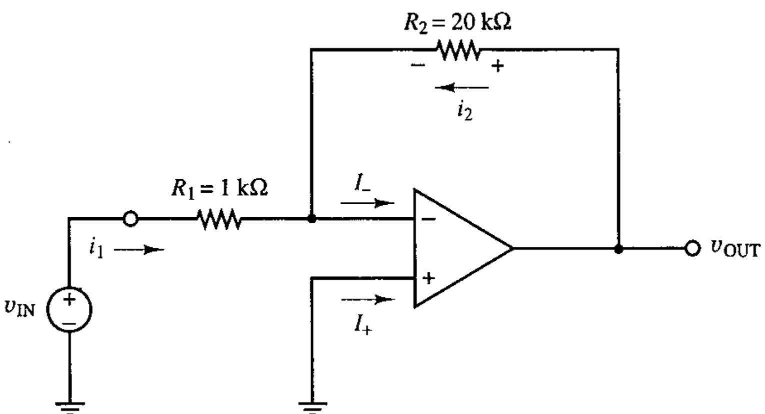


(b)

- A parameter called the **output-offset voltage** may be used to represent the internal imbalance of an op-amp, rather than the input-offset voltage
  - The output-offset voltage is defined as the measured output voltage when the input terminals are shorted together, as shown at the left-top fig.
  - The output-offset voltage may be modeled by placing a voltage source $A_o V_{IO}$ in series with the output voltage source $A_o(v_+ - v_-)$
    - Consequently, the output-offset voltage is essentially the input-offset voltage multiplied by the open loop gain.
  - Do exercise 2.34
- How can we correct for offset voltage?
  - Some op-amps provide two terminals (offset-null terminals) for adjusting out the offset voltage
    - A potentiometer is connected across the offset null terminals with the V_{NEG} supply voltage connected to the adjustable center tap
  - If the op-amp does not have an internal null adjustment provision, an external adjustment similar to that shown in Example 2.11 can be provided.
- Look at Exercise 2.36 (error in text)

Effect of Non-zero Input Bias Currents





- In practice op-amps do not actually have zero input currents, but rather have very small input currents labeled I_+ and I_- in the figure at the left
  - Modeled as internal current sources inside op-amp
  - I_+ and I_- are both the same polarity
    - e.g. if the input transistors are NPN bipolar devices, positive I_+ and I_- are required to provide base current
  - In order to allow for slightly different values of I_+ and I_-, we define the term I_{BIAS} as the average of I_+ and I_-

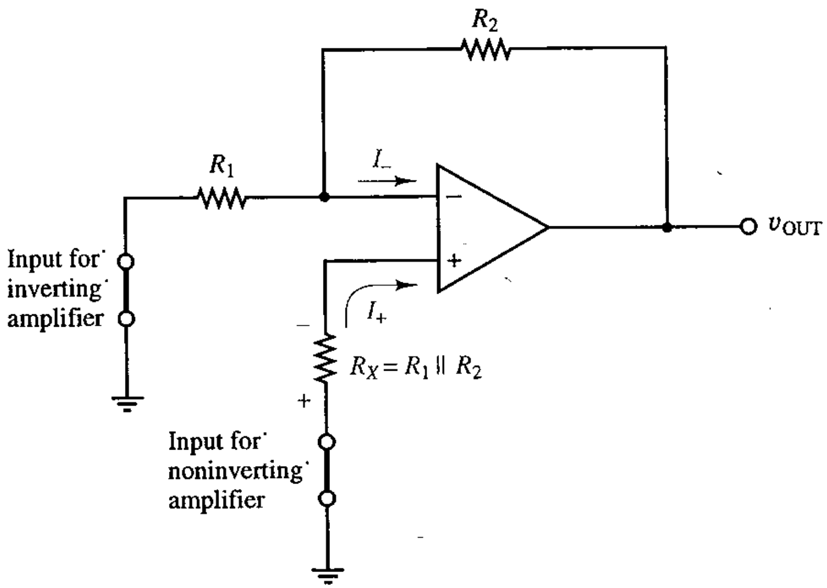
$$\mathbf{I_{BIAS} = ½ (I_+ + I_-)}$$

- Example: Given the op-amp shown in the bottom left figure, derive an expression for v_{out} that includes the effect of input bias currents
  - Assume $I_+ = I_- = 100$ nA
  - Using the virtual short condition and KCL, we can write $v_{IN}/R1 = I_- + (0-v_{OUT})/R2$ or

$$\mathbf{v_{OUT} = - (R_2/R_1)v_{IN} + I_-R_2}$$

  - Plugging in values gives $v_{OUT} = - 20\ v_{IN} + 2$ mV
  - Do exercise 2.38, p. 77

Correcting for Non-zero Input Bias Current



- The effect of non-zero input bias current can be zero'ed out by inserting a resistor R_x in series with the V+ input terminal (as shown)
  - This same correction works for both inverting and non-inverting op-amps
  - We choose Rx such that the dc component on the output caused by I+ exactly cancels the dc component on v_{OUT} caused by I-
  - One can use either KCL (Kirchhoff's Current Law) or superposition to show that choosing Rx = R1 || R2 completely cancels out the dc effect of non-zero input bias current
- KCL Method (inverting op-amp at left)
  - v_{IN} is applied to R1 and Rx is grounded
  - $v_- = v_+ = 0 - I_+ R_x$ due to virtual short
  - Apply KCL to v+ input:

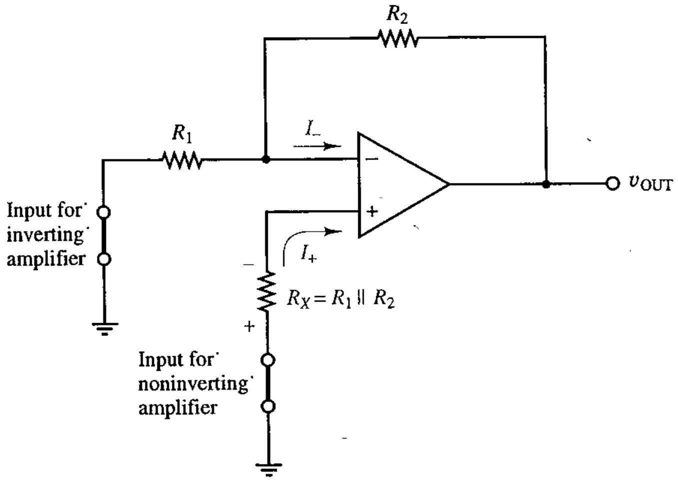
    $(v_{IN} - v_-)/R1 = I_- + (v_- - v_{OUT})/R2$
  - Solve for v_{OUT} and substitute $-I_+R_x$ for v_-

$v_{OUT} = -(R2/R1)\, v_{IN} + I_- R2 - I_+ R_x (R1 + R2)/R1$

  - Setting the dc bias terms equal yields

    Rx = R1 || R2 = R1 R2/(R1 + R2)

Input Offset Current Definition



- Non-zero input bias currents I+ and I- may not always be equal (some opamps)
  - Variation in bipolar transistor beta may cause base currents to non-track, or perhaps there are circuit design issues causing non equal offset I
- We define a parameter “input offset current”

  $\mathbf{I_{IO} = I_+ - I_-}$
  - Typical values of I_{IO} are 5-10% (of I-) although it can be as high as 50%
- Example 2.13 based on figure at left
  - R1 = 1K, R2 = 20K ohms
  - Assuming Ibias = 1 uA and I_{IO} = 100 nA, find I+, I-, and the effect of I_{IO} on vout
  - Since $(I_+ + I_-)/2$ = 1 uA and $I_+ - I_-$ = 0.1uA, we can solve for I+ = 1.05 uA and I- = 0.95 uA
  - Using the expression for Vout from slide 2-26 with Vin = 0 and Rx = R1 || R2 gives us
  - $v_{OUT} = R2\,(I_- - I_+) = -I_{IO}\,R2 = -2$ mV
- Do Exercise 2.40

Slew Rate Limitation in an Op-amp

- A real op-amp is limited in its ability to respond instantaneously to an input signal with a high rate of change of its input voltage. This limitation is called the **slew rate**, referring to the maximum rate at which the output can be "slewed".
  - Typical slew rates may be between 1–10 V/μs = 1E6 – 1E7 V/s
  - Max slew rate is a function of the device performance of the op-amp components & design
  - If the input is driven above the slew rate limit, the output will exhibit non-linear distortion
- Slew rate limitation behavior: (Example 2.14):
  - Assume an inverting op-amp with a gain of –10 has a max slew rate of 1 V/μs and is driven by a sinusoidal input with a peak of 1V. At what input frequency will the output start to show slew rate limitation?
    - Output has a peak of 10 volts since gain is –10 and input peak is 1 volt
    - If the input is given by v_{IN} = Vo sin ωt, the max slope will occur at t=0 and will be given by

      $$d(V_o \sin \omega t)/dt\,|(t=0) = \omega V_o = 2\pi f V_o$$
  - The max frequency is therefore given by

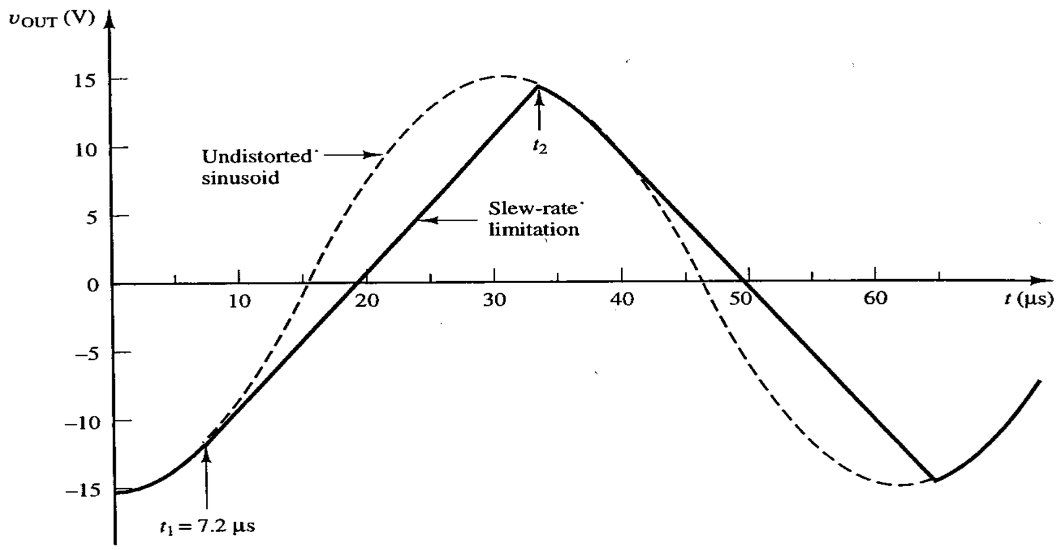
    $$\mathbf{f_{max} = slew\ rate/2\pi V_o} = 1E6\ V/s\ /\ 2\pi\ 10V = \sim 16\ kHz$$
  - Note: This surprisingly low max frequency is directly proportional to the slew rate limit spec and inversely proportional to the peak output voltage!

Slew Rate Limitation in an Op-amp

Exceeding the slew rate limitation (Example 2.14b):

- If the inverting op-amp from 2.14a (with gain = –10 and slew rate = 1 V/μs) is driven by a 16 kHz sinusoidal input with a peak of 1.5V, what is the effect on the output waveform?
  - Since we are now exceeding the slew rate limit, the output will be distorted
  - Let v_{OUT} = - Vo cos ωt (for visual simplicity) where Vo = 10 x 1.5V = 15V
  - Then $dv_{OUT}/dt = \omega V_o \sin \omega t$
  - Above some t = t_1 the slew rate will limit the output response

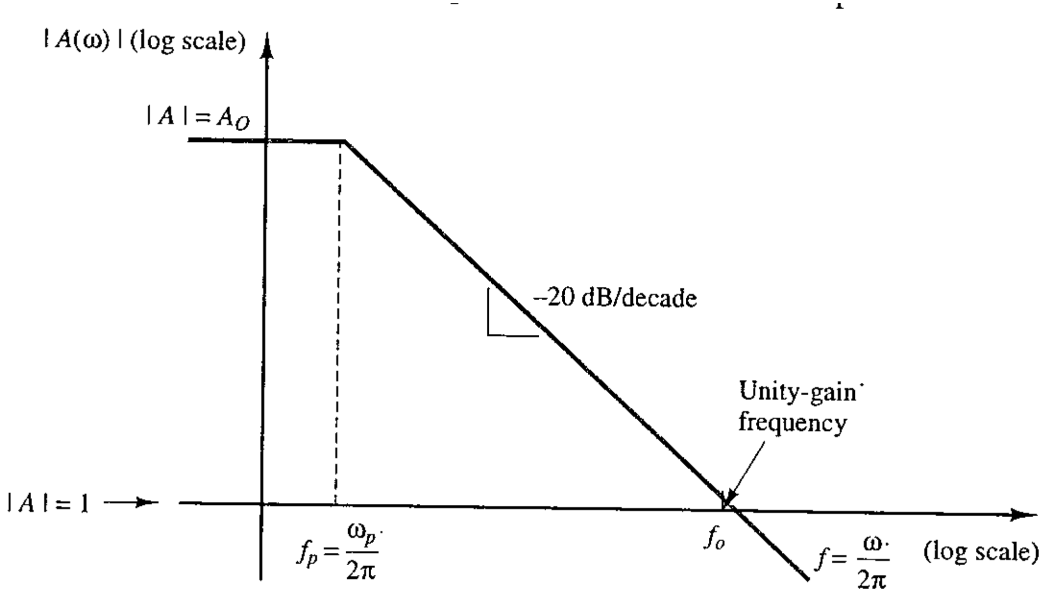
    $t_1 = (1/\omega) \sin^{-1}$ (slew rate/ωVo) = (1/2π 16 kHz) $\sin^{-1}$ (1E6 /2π 16 kHz x 15V) = 7.2 μs
  - The resulting waveform is shown below. At t_1 the slew-limited output can't keep up with the input until it catches up at t_2, when the cycle starts all over again.



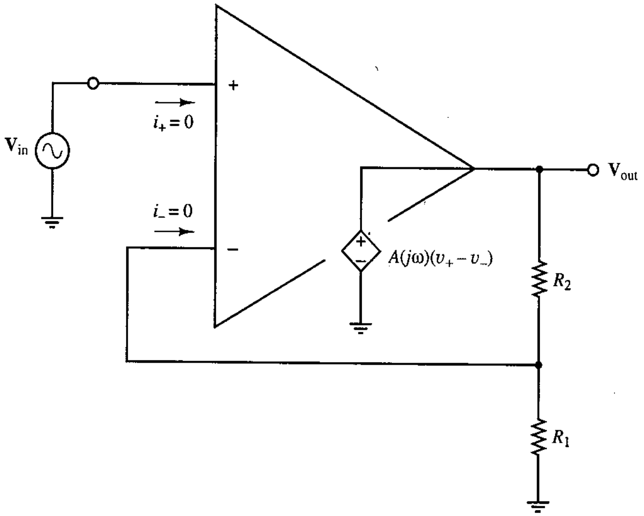
Frequency Response of an Op-amp

- An open-loop op-amp has a constant gain Ao only at low frequencies, and a continuously reducing gain at higher frequencies due to internal device and circuit inherent limits.
  - For a single dominant pole at freq f_p, the frequency-dependent gain $A(j\omega)$ can be written as

    $\mathbf{A(j\omega) = Ao/[1 + j\omega/\omega_p] = Ao/[1 + jf/ f_p]}$ where $\omega_p = 2\pi f_p$
  - the gain rolls off at 20dB/decade for frequencies above f_p, as shown below
- An op-amp may have additional higher frequency poles, as well, but is often described over a large frequency range by the dominant pole (as assumed in the figure below)
- The unity gain frequency f_o is defined as the frequency where the gain = 1
  - For the single dominant pole situation assumed in the figure below, f_o can be found by extrapolating the 20 dB/decade roll-off to the point where the gain is unity.



Frequency-Dependent Closed-Loop Gain



- The effect of the frequency-dependent open-loop gain on the closed-loop gain can easily be found by deriving $v_{OUT}(j\omega)$ as a function of the open-loop gain $A(j\omega)$ in the op-amp configuration shown at the left

  $v_{OUT} = A(j\omega)\ (v+ - v-)$

  $= A(j\omega)\ [v_{IN} – v_{OUT}(R1/(R1 + R2))]$, or

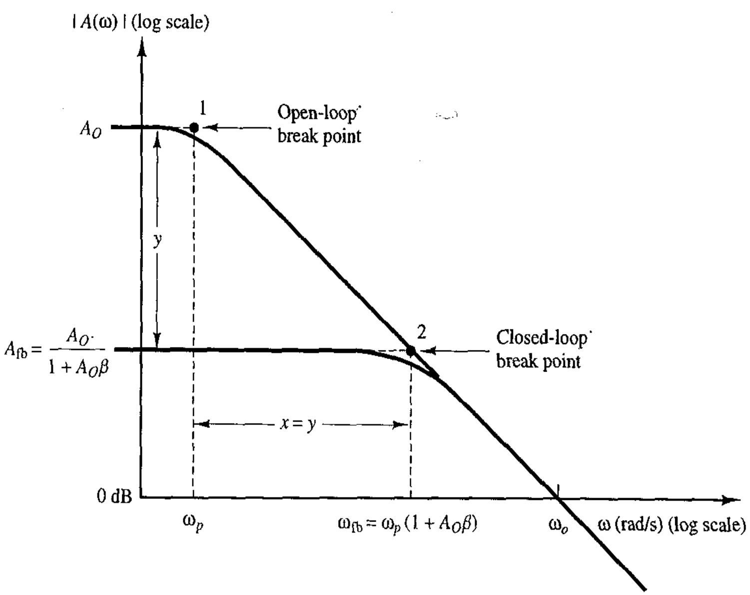
  $\mathbf{v_{OUT} = A(j\omega)/[1 + A(j\omega)\beta]}$ where

  $\beta = R1 / (R1 + R2)$ is the closed-loop feedback function

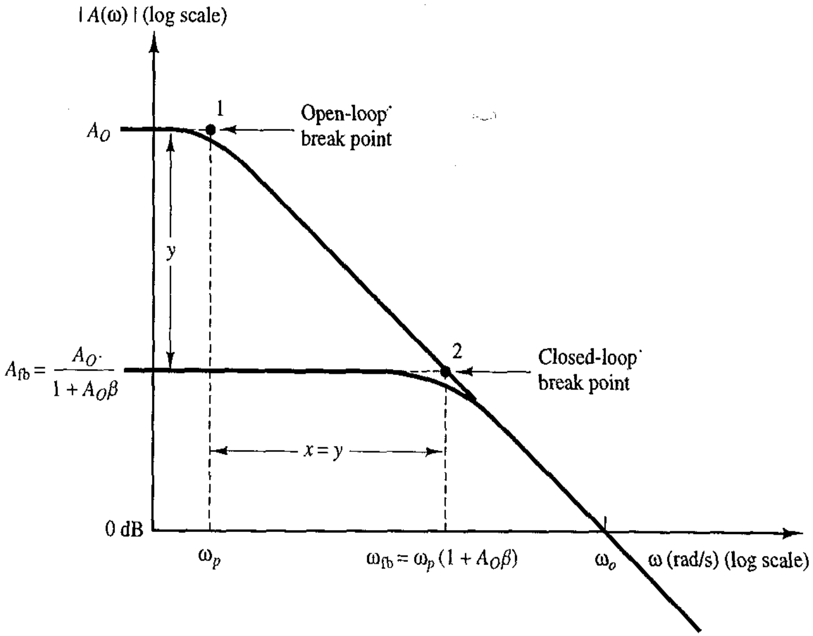
  – Substituting A(jw) into the above equation gives us the complete frequency dependent result for the closed loop gain

  $$\mathbf{v_{OUT}/v_{IN} = Ao/[1 + Ao\beta + j\omega/\omega_p]}$$
  $$\mathbf{= [Ao/(1 + Ao\beta)]/[1 + j\omega/\omega_p(1 + Ao\beta)]}$$

- The dc gain is given by
  – $Ao/(1 + Ao\beta) = \sim 1/\beta = (R1 + R2)/R1$
- The closed-loop response is seen to contain a single pole at $\omega_{fb} = \omega_p(1 + Ao\beta) >> \omega_p$
  – **Closed-loop BW = ~ $A_o\beta$ x open-loop BW**



Gain-Bandwidth Product



- Multiplication of the closed-loop BW by the closed-loop gain gives us

  $$[Ao/(1+Ao\beta)]\omega_{fb} = [Ao/(1+Ao\beta)]\omega_p(1+Ao\beta)$$
  $$= Ao\omega_p$$

  - which is the open-loop gain-BW product
- For the assumption of a single dominant pole and very high Ao, the gain-bandwidth product is a constant
- Unity-gain frequency ω_o (= $2\pi f_o$) is the freq where the op-amp response extrapolates to a gain of 1
  - we can show that $\omega_o = A_o\omega_p$ (for a system with a single dominant pole)

Op-amp Output Current Limit:

- A typical op-amp contains circuitry to limit the output current to a specified maximum in order to protect the output stage from damage
  - If a low value load impedance is utilized, the output current limit may be reached before the output saturates at the rail voltage, forcing the op-amp to lower gain
  - See Example 2.15

Nonlinear Op-Amp Circuits

- Most typical applications require op amp and its components to act linearly
  - I-V characteristics of passive devices such as resistors, capacitors should be described by linear equation (Ohm's Law)
  - For op amp, linear operation means input and output voltages are related by a constant proportionality (A_v should be constant)
- Some application require op amps to behave in nonlinear manner (logarithmic and antilogarithmic amplifiers)

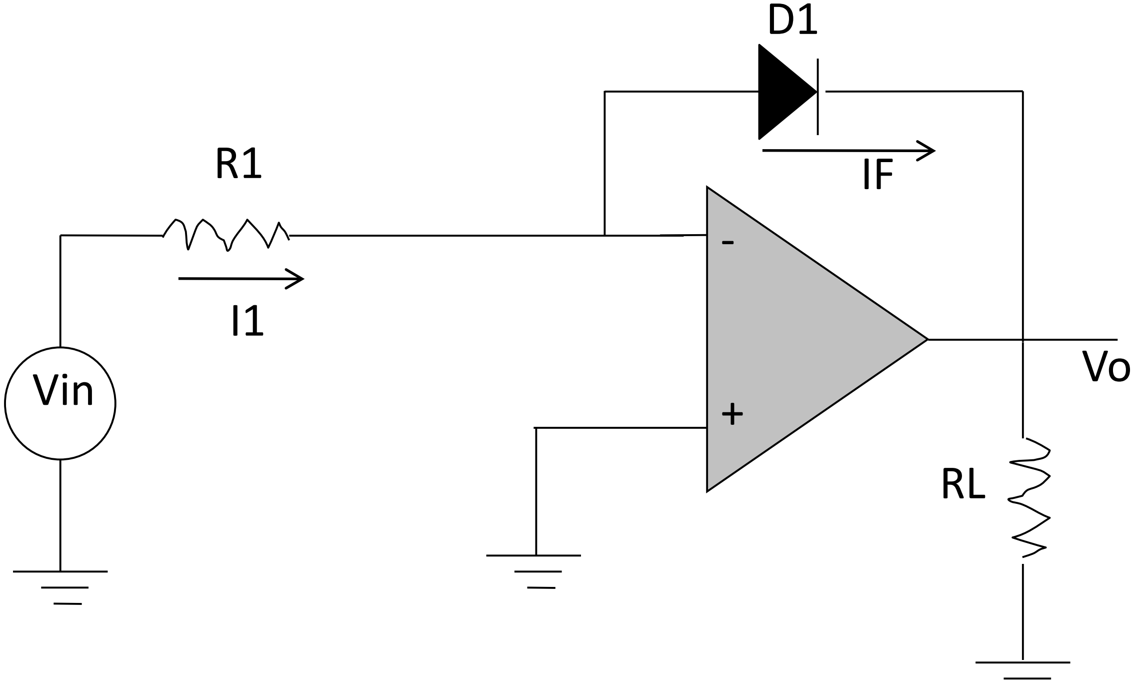
Logarithmic Amplifier

- Output voltage is proportional to the logarithm of input voltage
- A device that behaves nonlinearly (logarithmically) should be used to control gain of op amp
  - Semiconductor diode
- Forward transfer characteristics of silicon diodes are closely described by Shockley's equation

  $I_F = I_s e^{(V_F/\eta V_T)}$

  - I_s is diode saturation (leakage) current
  - e is base of natural logarithms (e = 2.71828)
  - V_F is forward voltage drop across diode
  - V_T is thermal equivalent voltage for diode (26 mV at 20°C)
  - η is emission coefficient or ideality factor (2 for currents of same magnitude as I_S to 1 for higher values of I_F)

Basic Log Amp operation

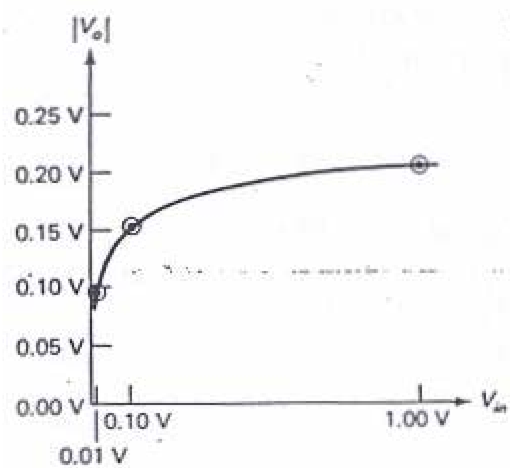


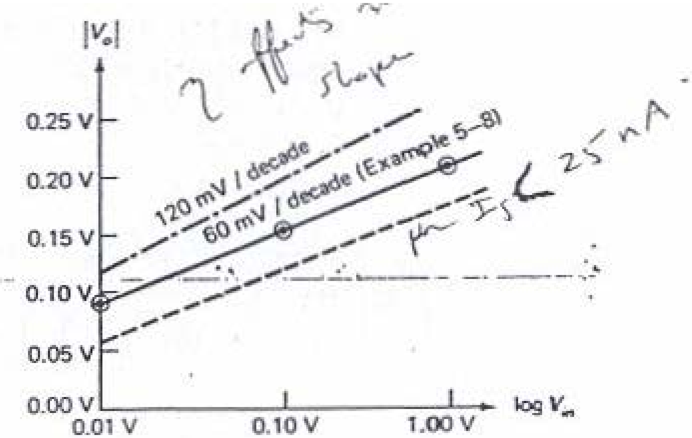
- $I1 = Vin/R1$
- $IF = - I1$
- $IF = - Vin/R1$
- $V0 = -VF = -\eta VT \ln(IF/IS)$
- $V0 = -\eta VT \ln[Vin/(R1IS)]$
- $rD = 26 \text{ mV} / IF$
- $IF < 1$ mA (log amps)

- At higher current levels ($IF > 1$ mA) diodes begin to behave somewhat linearly

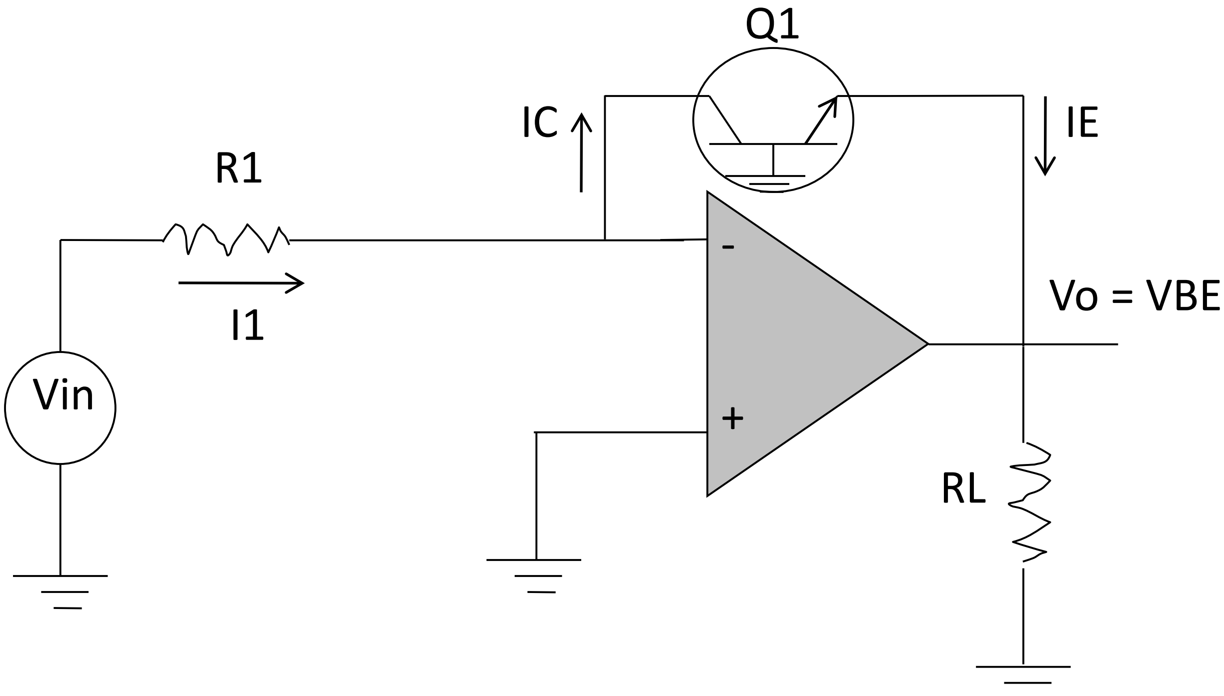
Logarithmic Amplifier

- Linear graph: voltage gain is very high for low input voltages and very low for high input voltages
- Semilogarithmic graph: straight line proves logarithmic nature of amplifier's transfer characteristic
- Transfer characteristics of log amps are usually expressed in terms of slope of V_0 versus V_{in} plot in milivolts per decode
- η affects slope of transfer curve; I_S determines the y intercept





Additional Log Amp Variations



$$IC = IESe^{(V_{BE}/V_T)}$$

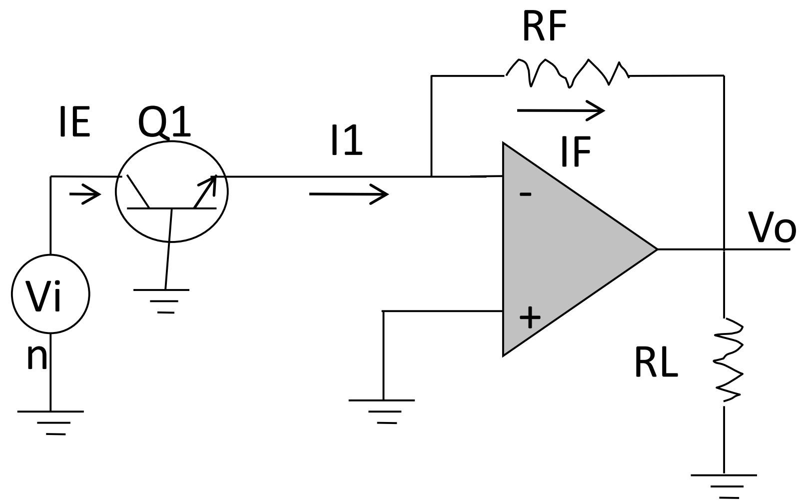
- IES is emitter saturation current
- VBE is drop across base-emitter junction

- Often a transistor is used as logging element in log amp (transdiode configuration)
- Transistor logging elements allow operation of log amp over wider current ranges (greater dynamic range)

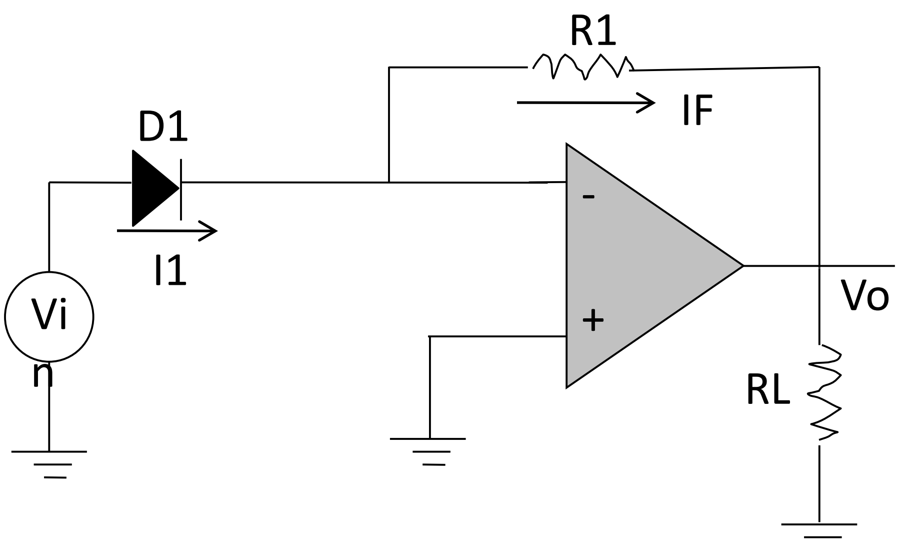
Antilogarithmic Amplifier

- Output of an antilog amp is proportional to the antilog of the input voltage
- with diode logging element
  - $V_0 = -R_F I_S e^{(V_{in}/V_T)}$
- With transdiode logging element
  - $V_0 = -R_F I_{ES} e^{(V_{in}/V_T)}$
- As with log amp, it is necessary to know saturation currents and to tightly control junction temperature

Antilogarithmic Amplifier



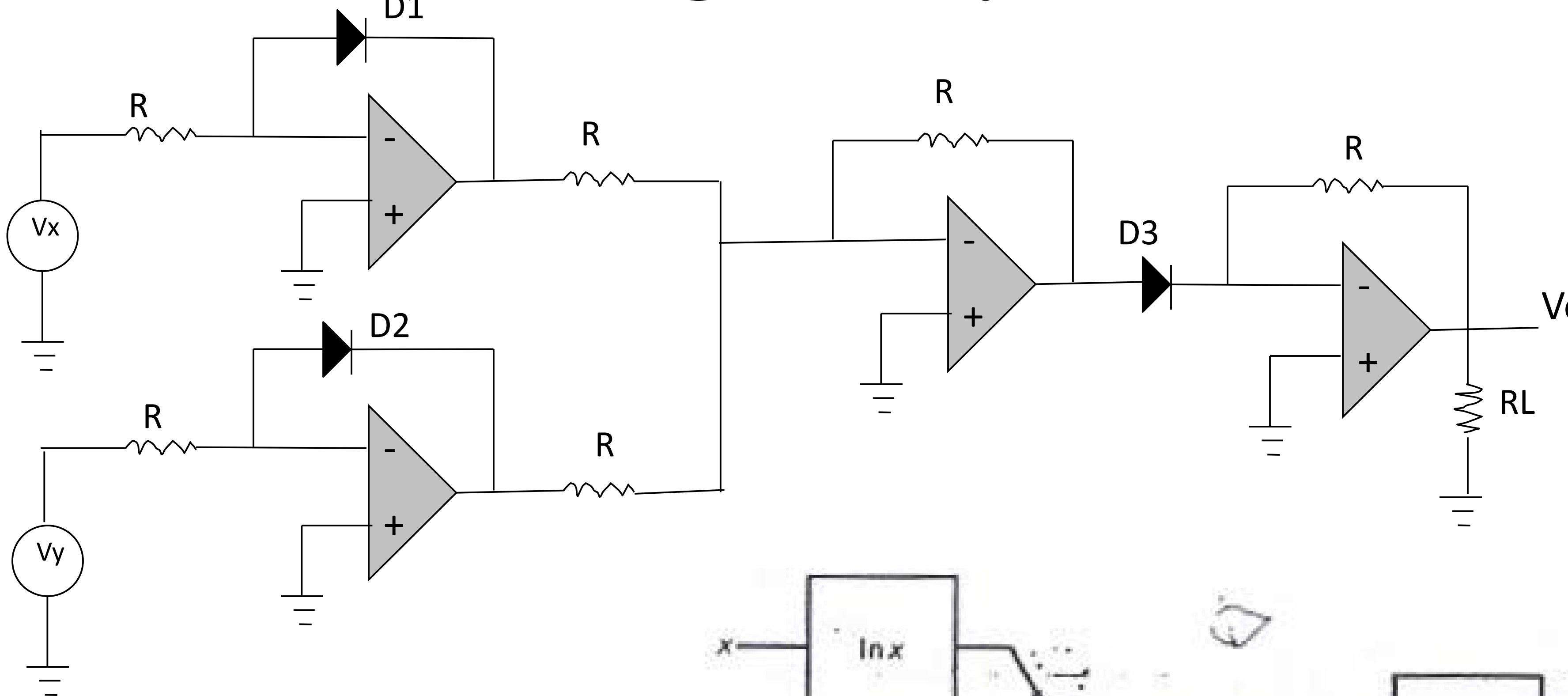
$(\alpha = 1)\ I1 = IC = IE$



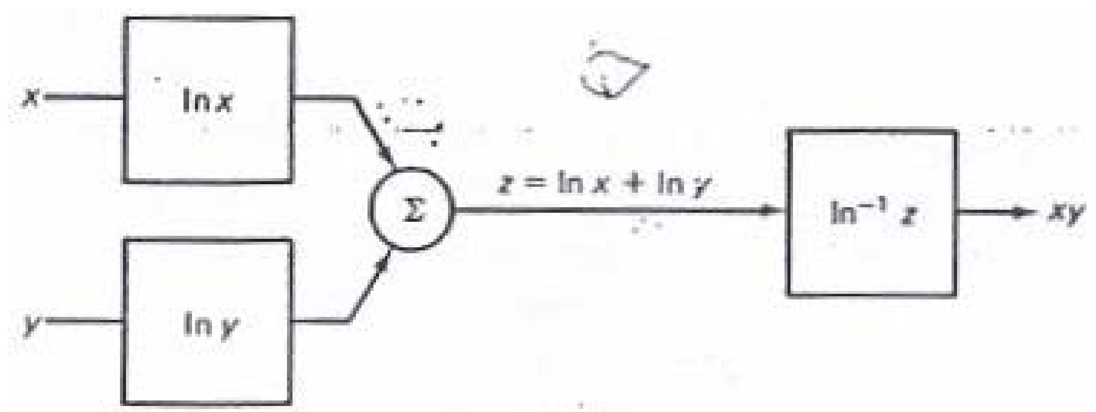
Logarithmic Amplifier Applications

- Logarithmic amplifiers are used in several areas
  - Log and antilog amps to form analog multipliers
  - Analog signal processing
- Analog Multipliers
  - $\ln xy = \ln x + \ln y$
  - $\ln (x/y) = \ln x - \ln y$

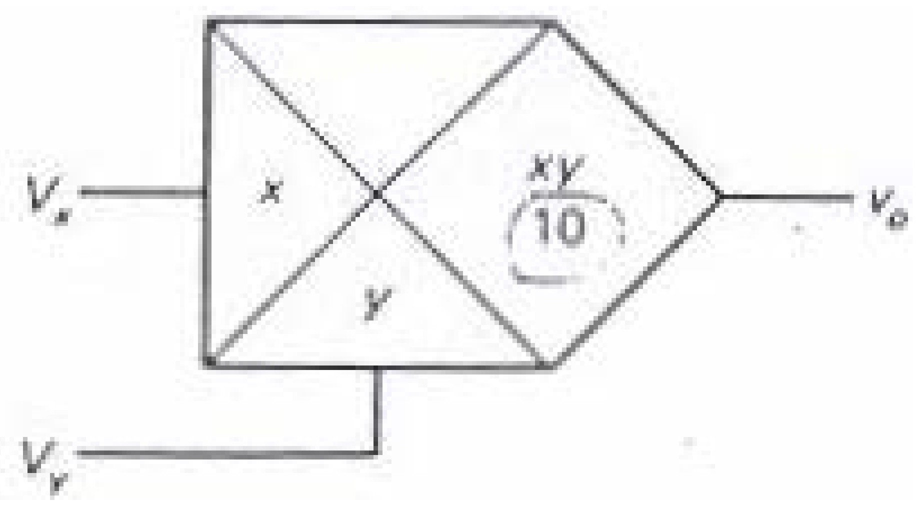
Analog Multipliers



One-quadrant multiplier: inputs must both be of same polarity

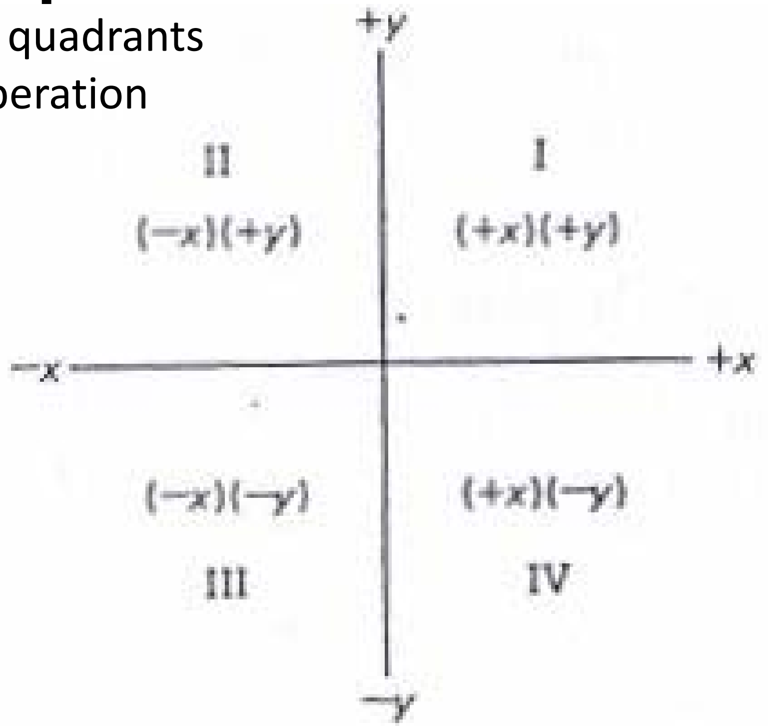


Analog Multipliers



General symbol

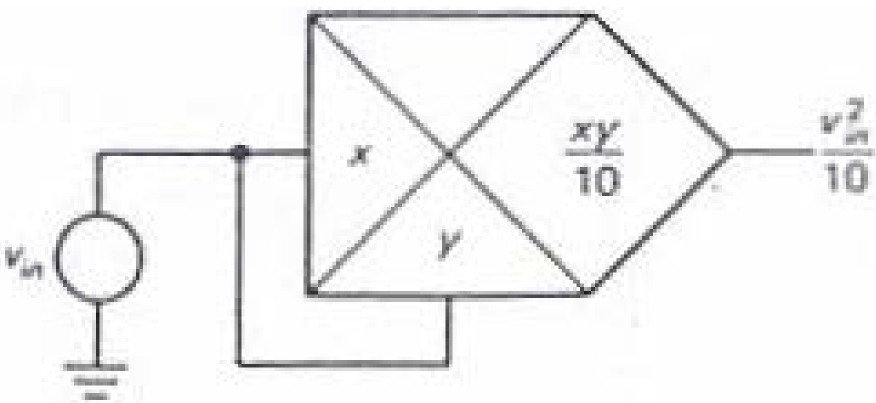
Four quadrants of operation



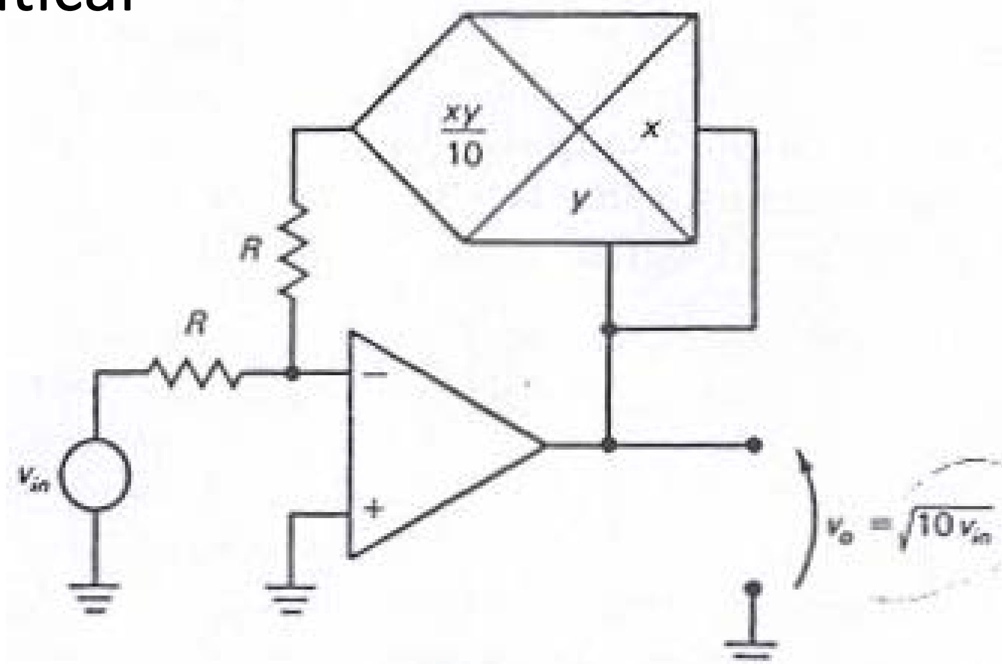
Two-quadrant multiplier: one input should have positive voltages, other input could have positive or negative voltages
Four-quadrant multiplier: any combinations of polarities on their inputs

Analog Multipliers

Implementation of mathematical operations



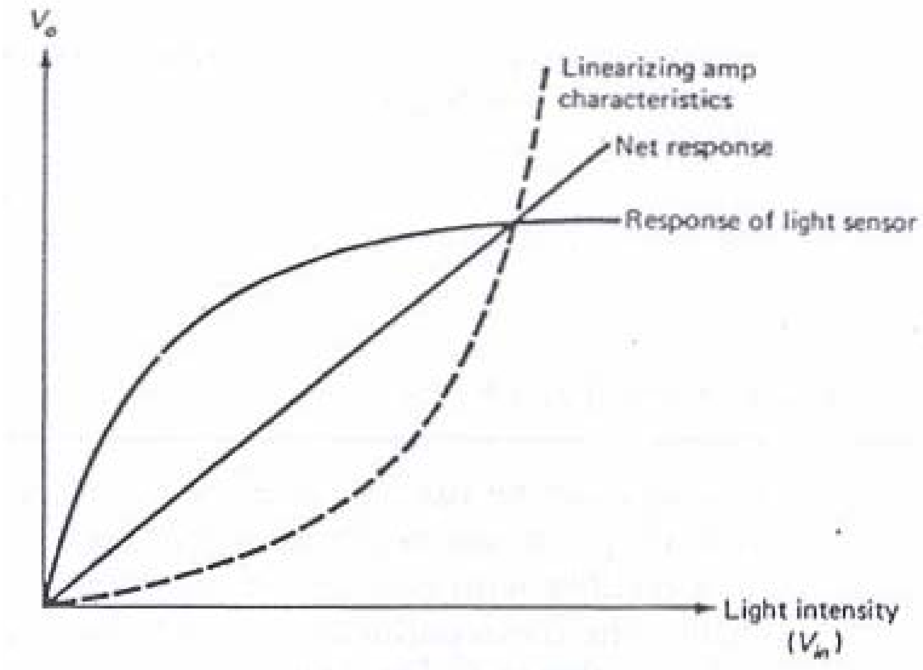
Squaring Circuit



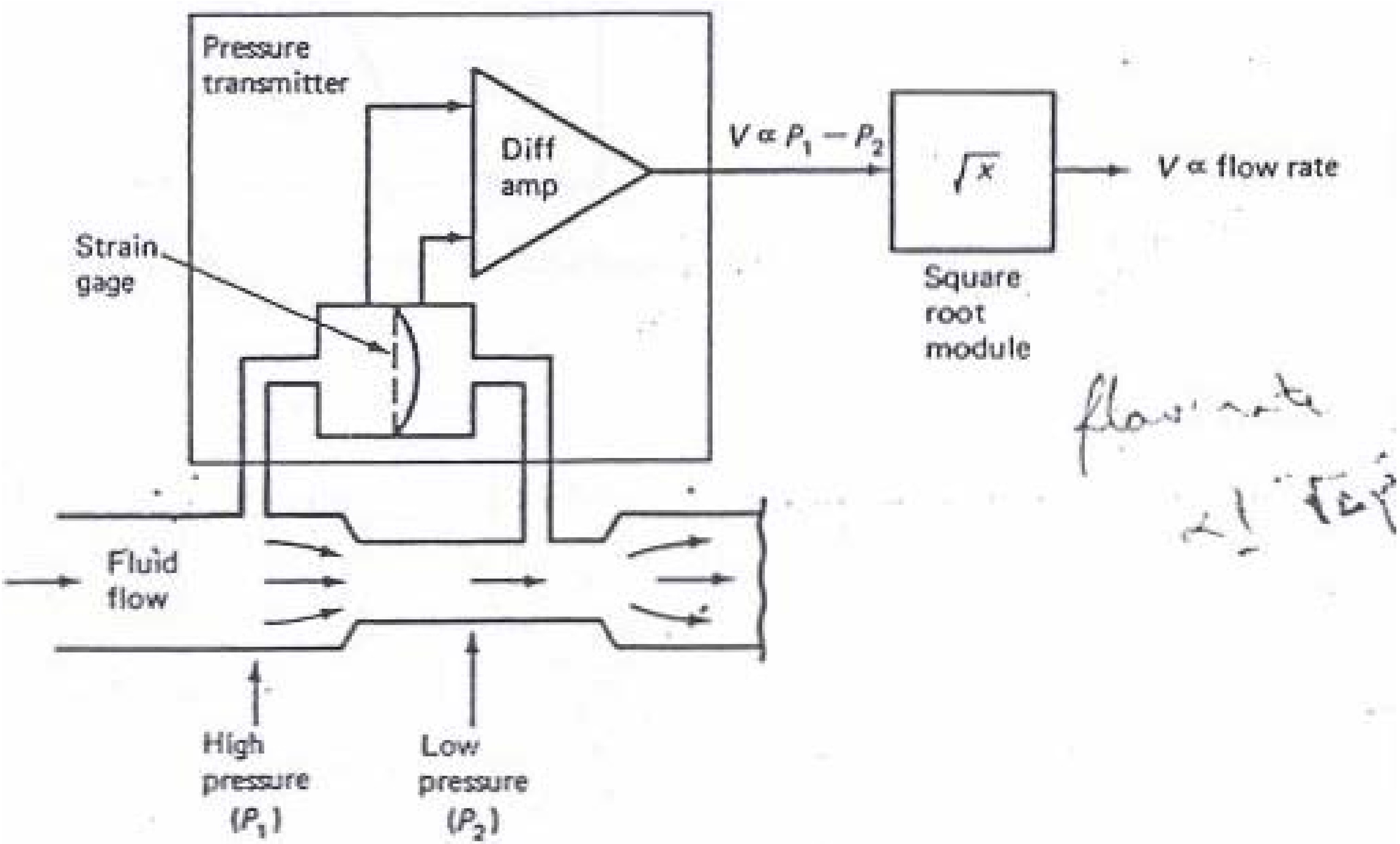
Square root Circuit

Signal Processing

- Many transducers produce output voltages that vary nonlinearly with physical quantity being measured (thermistor)
- Often It is desirable to linearize outputs of such devices; logarithmic amps and analog multipliers can be used for such purposes
- Linearization of a signal using circuit with complementary transfer characteristics



Pressure Transmitter



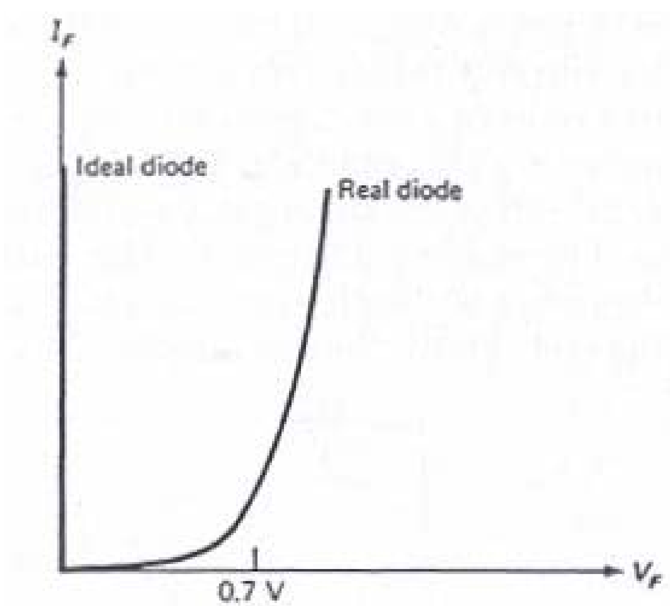
Pressure transmitter produces an output voltage proportional to difference in pressure between two sides of a strain gage sensor

Pressure Transmitter

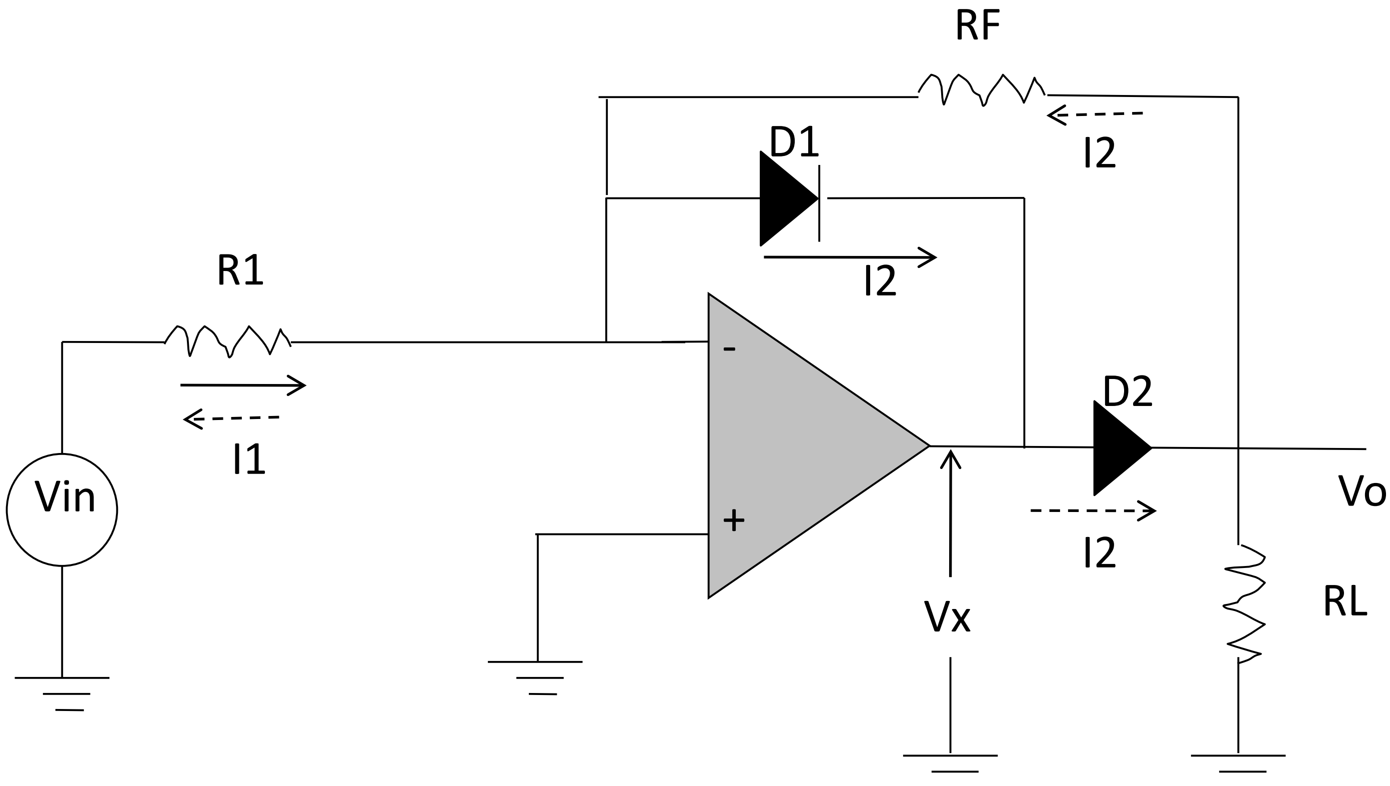
- A venturi is used to create pressure differential across strain gage
- Output of transmitter is proportional to pressure differential
- Fluid flow through pipe is proportional to square root of pressure differential detected by strain gage
- If output of transmitter is processed through a square root amplifier, an output directly proportional to flow rate is obtained

Precision Rectifiers

- Op amps can be used to form nearly ideal rectifiers (convert ac to dc)
- Idea is to use negative feedback to make op amp behave like a rectifier with near-zero barrier potential and with linear I/O characteristic
- Transconductance curves for typical silicon diode and an ideal diode

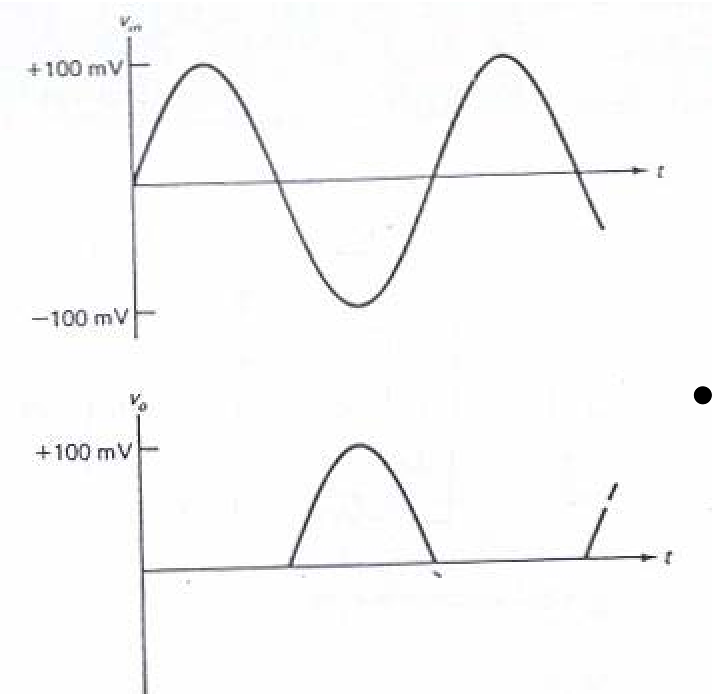


Precision Half-Wave Rectifier



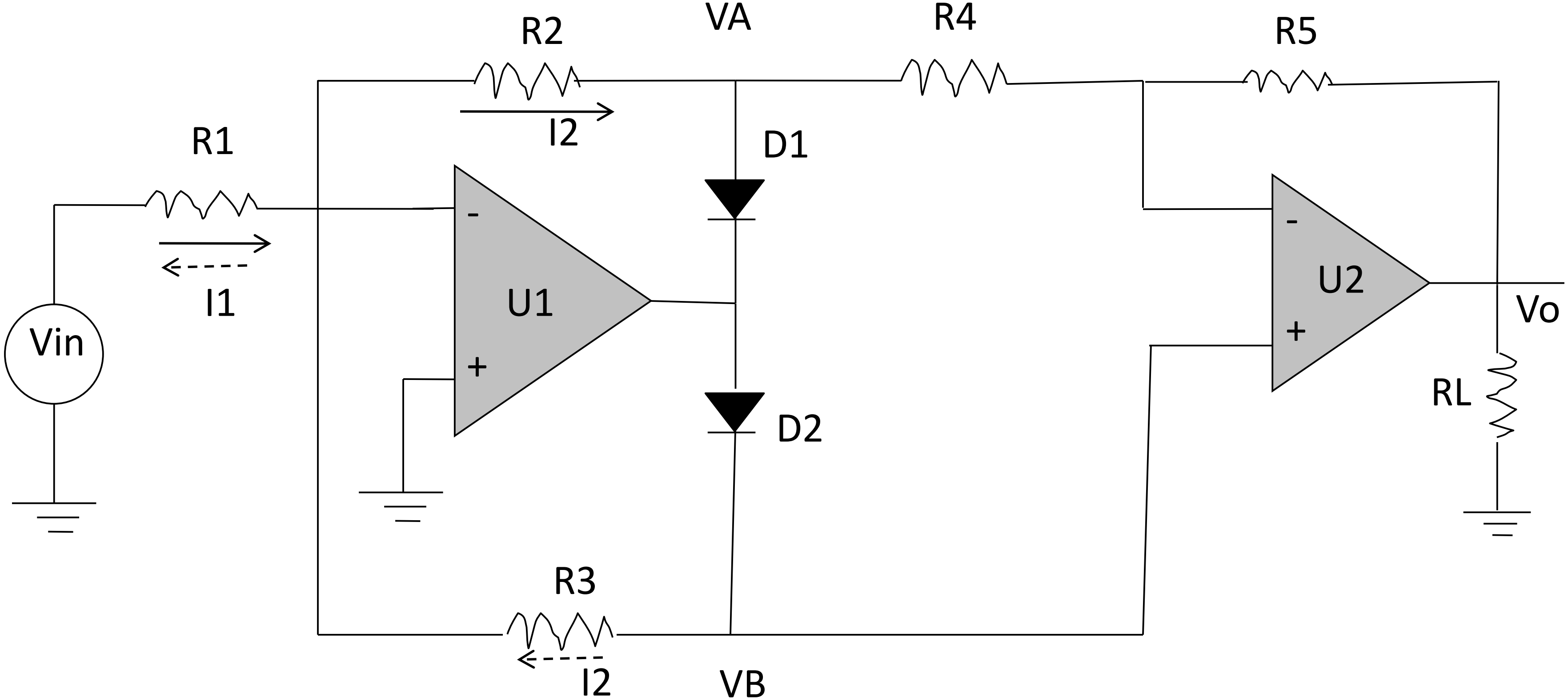
- Solid arrows represent current flow for positive half-cycles of V_{in} and dashed arrows represent current flow for negative half-cycles

Precision Half-Wave Rectifier



- If signal source is going positive, output of op amp begins to go negative, forward biasing D_1
  - Since D_1 is forward biased, output of op amp V_x will reach a maximum level of ~ -0.7V regardless of how far positive V_{in} goes
  - This is insufficient to appreciably forward bias D_2, and V_0 remains at 0V
- On negative-going half-cycles, D_1 is reverse-biased and D_2 is forward biased
  - Negative feedback reduces barrier potential of D_2 to $0.7V/A_{OL}$ (~ = 0)
  - Gain of circuit to negative-going portions of V_{in} is given by $A_V = -R_F/R_1$

Precision Full-Wave Rectifier



- Solid arrows represent current flow for positive half-cycles of V_{in} and dashed arrows represent current flow for negative half-cycles

Precision Full-Wave Rectifier

- Positive half-cycle causes D_1 to become forward-biased, while reverse-biasing D_2
  - $V_B = 0$ V
  - $V_A = -V_{in} R_2/R_1$
  - Output of U_2 is $V_0 = -V_A R_5/R_4 = V_{in} (R_2R_5/R_1R_4)$
- Negative half-cycle causes U_1 output positive, forward-biasing D_2 and reverse-biasing D_1
  - $V_A = 0$ V
  - $V_B = -V_{in} R_3/R_1$
  - Output of U_2 (noninverting configuration) is $V_0 = V_B [1+ (R_5/R_4)]= - V_{in} [(R_3/R_1)+(R_3R_5/R_1R_4)$
  - if $R_3 = R_1/2$, both half-cycles will receive equal gain

Precision Rectifiers

- Useful when signal to be rectified is very low in amplitude and where good linearity is needed
- Frequency and power handling limitations of op amps limit the use of precision rectifiers to low-power applications (few hundred kHz)
- Precision full-wave rectifier is often referred to as absolute magnitude circuit

ACTIVE FILTERS

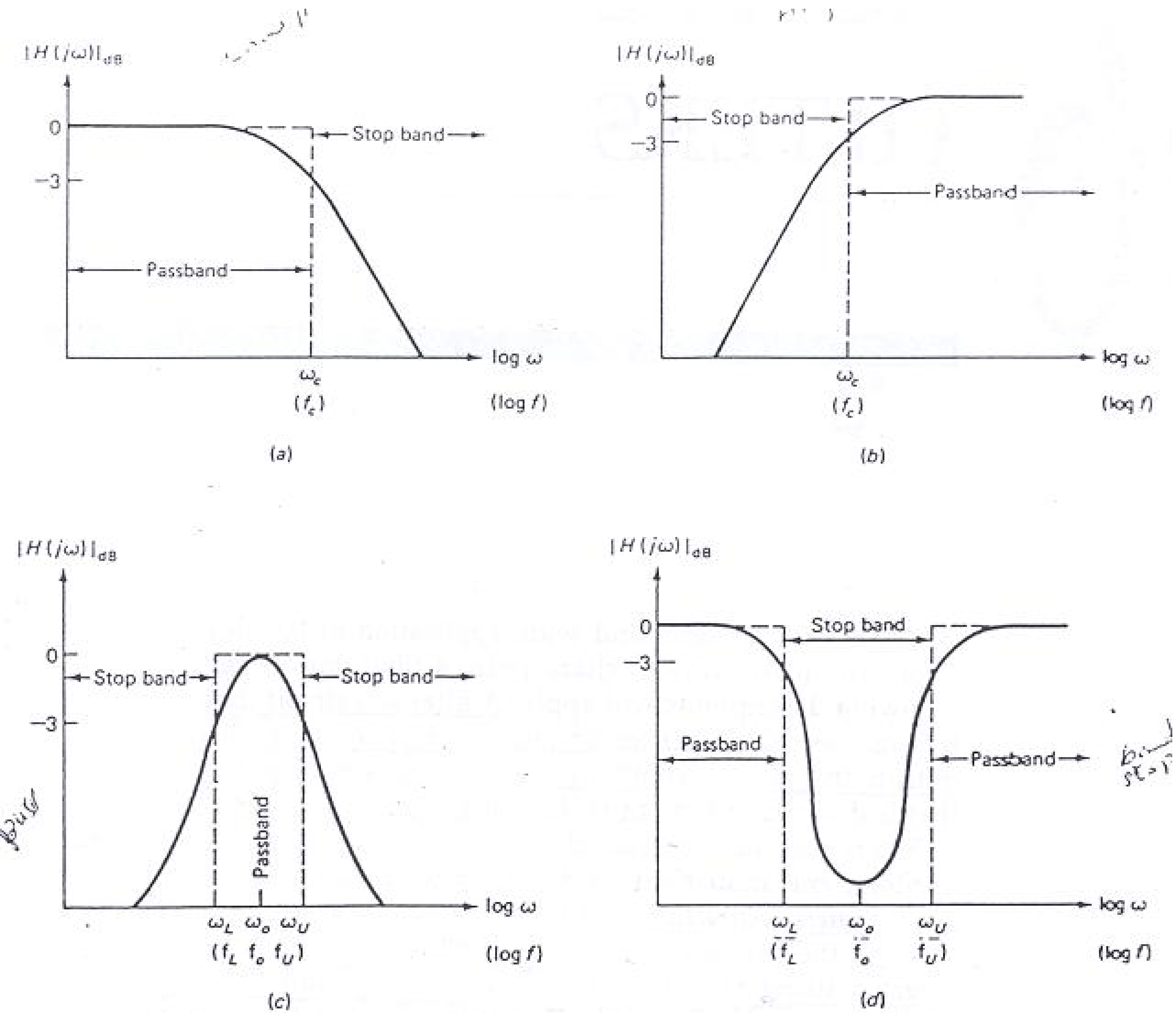
Active Filters

- Op amps have wide applications in design of active filters
- Filter is a circuit designed to pass frequencies within a specific range, while rejecting all frequencies that fall outside this range
- Another class of filters are designed to produce an output that is delayed in time or shifted in phase with respect to filter's input
- Passive filters: constructed using only passive components (resistors, capacitors, inductors)
- Active filters: characteristics are augmented using one or more amplifiers; constructed using op amps, resistors, and capacitors only
  - Allow many filter parameters to be adjusted continuously and at will

Filter Fundamentals

- Five basic types of filters
  - Low-pass (LP)
  - High-pass (HP)
  - Bandpass (BP)
  - Bandstop (notch or band-reject)
  - All-pass (or time-delay)

Response Curves



- ω is in rad/s
- l H(jω) l denotes frequency-dependent voltage gain of filter
- Complex filter response is given by

H(jω) = l H(jω) l <θ(jω)

- If signal frequencies are expressed in Hz, filter response is expressed as l H(jf) l

Filter Terminology

- Filter passband: range of frequencies a filter will allow to pass, either amplified or relatively unattenuated
- All other frequencies are considered to fall into filter's stop band(s)
- Frequency at which gain of filter drops by 3.01 dB from that of passband determines where stop band begins; this frequency is called corner frequency (f_c)
- Response of filter is down by 3 dB at corner frequency (3 dB decrease in voltage gain translates to a reduction of 50% in power delivered to load driven by filter)
- f_c is often called half-power point

Filter Terminology

- Decibel voltage gain is actually intended to be logarithmic representation of power gain
- Power gain is related to decibel voltage gain as
  - $A_P = 10 \log (P_0/P_{in})$
  - $P_0 = (V_0^2/Z_L)$ and $P_{in} = (V_{in}^2/Z_{in})$
  - $A_P = 10 \log [(V_0^2/Z_L) /(V_{in}^2/Z_{in})]$
  - $A_P = 10 \log (V_0^2 Z_{in} /V_{in}^2 Z_L)]$
  - If $Z_L = Z_{in}$, $A_P = 10 \log (V_0^2/V_{in}^2) = 10 \log (V_0/V_{in})^2$
  - $A_P = 20 \log (V_0/V_{in}) = 20 \log A_v$
- When input impedance of filter equals impedance of load being driven by filter, power gain is dependent on voltage gain of circuit only

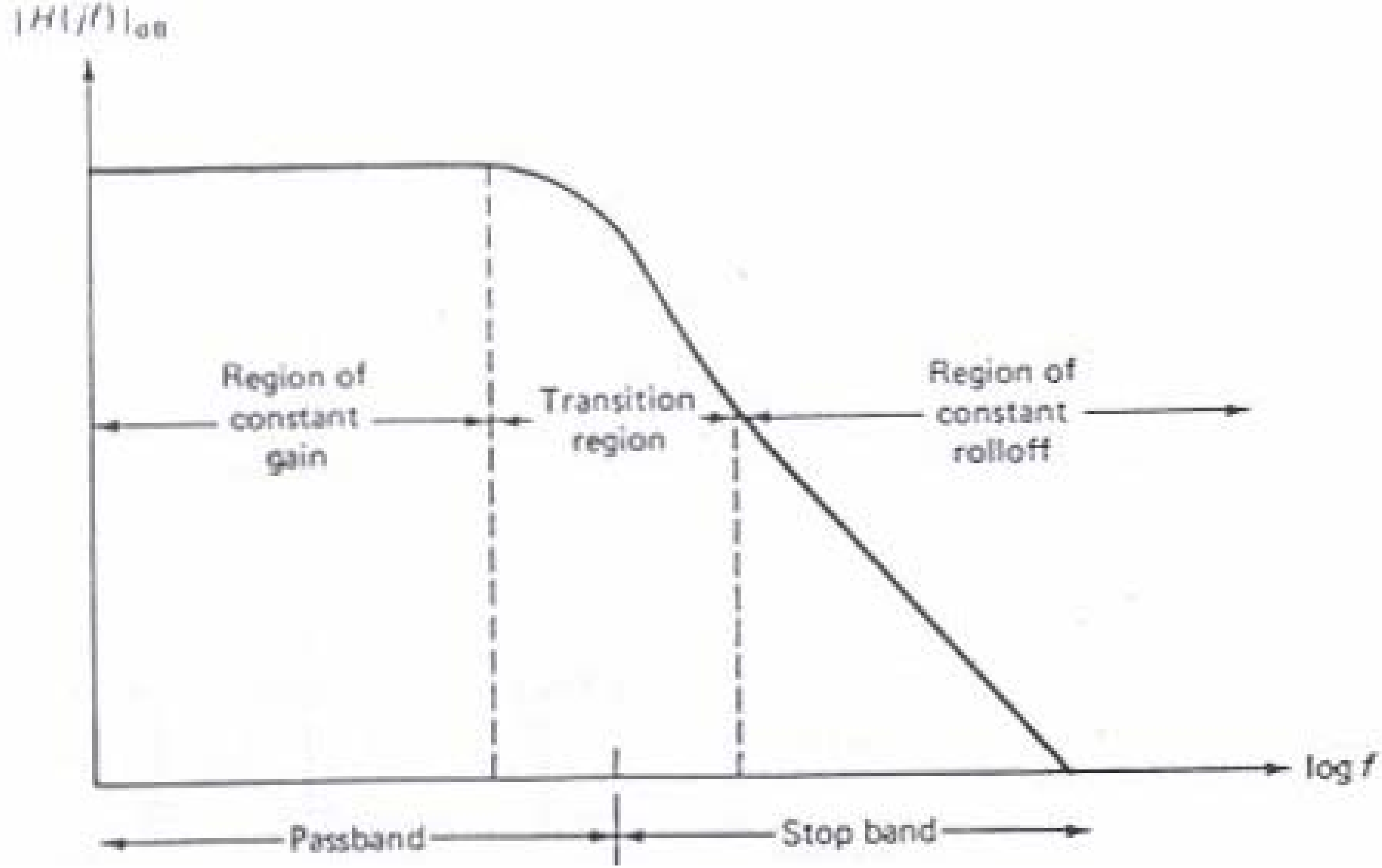
Filter Terminology

- Since we are working with voltage ratios, gain is expressed as voltage gain in dB
  - $| H(j\omega) |_{dB} = 20 \log (V_0/V_{in}) = 20 \log A_V$
- Once frequency is well into stop band, rate of increase of attenuation is constant (dB/decade rolloff)
- Ultimate rolloff rate of a filter is determined by order of that filter
- 1^{st} order filter: rolloff of -20 dB/decade
- 2^{nd} order filter: rolloff of -40 dB/decade
- General formula for rolloff = -20n dB/decade (n is the order of filter)
- Octave is a twofold increase or decrease in frequency
- Rolloff = -6n dB/octave (n is order of filter)

Filter Terminology

- Transition region: region between relatively flat portion of passband and region of constant rolloff in stop band
- Give two filter of same order, if one has a greater initial increase in attenuation in transition region, that filter will have a greater attenuation at any given frequency in stop band
- Damping coefficient (α): parameter that has great effect on shape of LP or HP filter response in passband, stop band, and transition region (0 to 2)
- Filters with lower α tend to exhibit peaking in passband (and stopband) and more rapid and radically varying transition-region response attenuation
- Filters with higher α tend to pass through transition region more smoothly and do not exhibit peaking in passband and stopband

LP Filter Response



Filter Terminology

- HP and LP filters have single corner frequency
- BP and bandstop filters have two corner frequencies (f_L and f_U) and a third frequency labeled as f_0 (center frequency)
- Center frequency is geometric mean of f_L and f_U
- Due to log f scale, f_0 appears centered between f_L and f_U

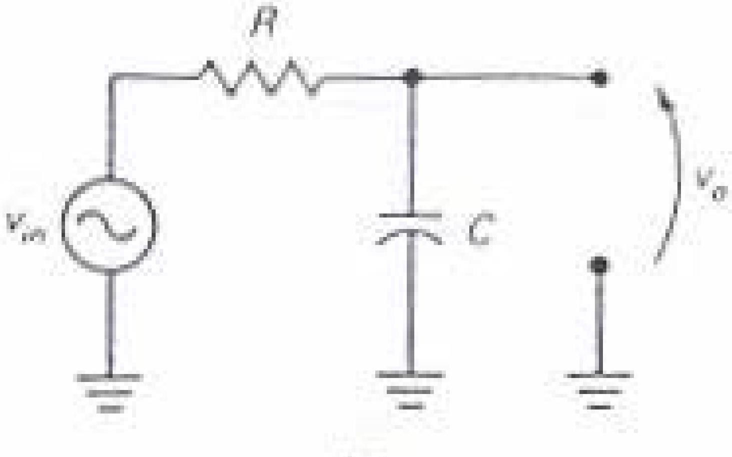
$$f_0 = \text{sqrt}\ (f_L f_U)$$

- Bandwidth of BP or bandstop filter is

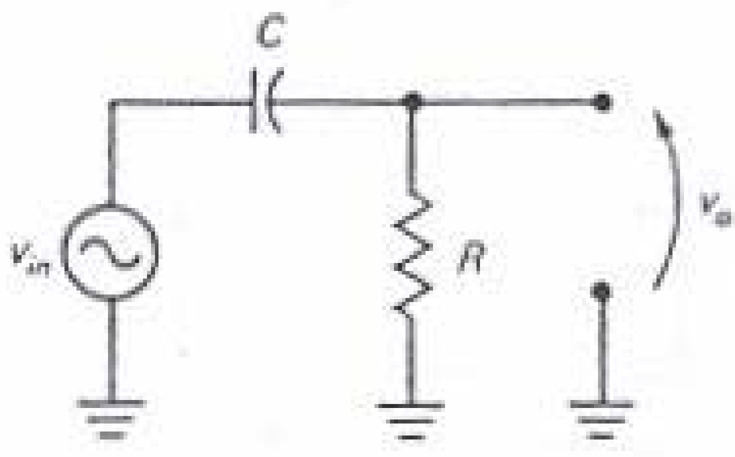
$$BW = f_U - f_L$$

- Also, $Q = f_0 / BW$ (BP or bandstop filters)
- BP filter with high Q will pass a relatively narrow range of frequencies, while a BP filter with lower Q will pass a wider range of frequencies
- BP filters will exhibit constant ultimate rolloff rate determined by order of the filter

Basic Filter Theory Review



(a)



(b)

- Simplest filters are 1st order LP and HP RC sections
  - Passband gain slightly less than unity
- Assuming neglegible loading, amplitude response (voltage gain) of LP section is

  $H(j\omega) = (jX_C) / (R + jX_C)$

  $H(j\omega) = X_C/\mathrm{sqrt}(R^2+X_C^2) < -\tan^{-1} (R/X_C)$
- Corner frequency f_c for 1st order LP or HP RC section is found by making $R = X_C$ and solving for frequency

  $R = X_C = 1/(2\pi fC)$

  $1/f_C = 2\pi RC$

  $f_C = 1/(2\pi RC)$
- Gain (in dB) and phase response of 1st order LP

  $H(jf)\ \mathrm{dB} = 20 \log [1/\{\mathrm{sqrt}(1+(f/f_c)^2\}] < -\tan^{-1} (f/f_C)$
- Gain (in dB) and phase response of 1st order HP

  $H(jf)\ \mathrm{dB} = 20 \log [1/\{\mathrm{sqrt}(1+(f_c/f)^2\}] < \tan^{-1} (f_C/f)$